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CENTRE NATIONAL D'ÉTUDES SPATIALES

DEALING WITH RADIATIVE ENVIRONMENT

THE MOST UNPREDICTABLE ATTACKER IN SPACE

BITFLIP CONFERENCE – RENNES - FRANCE

Florent MANNI (CNES- DTN/TVO/ET)
florent.manni@cnes.fr

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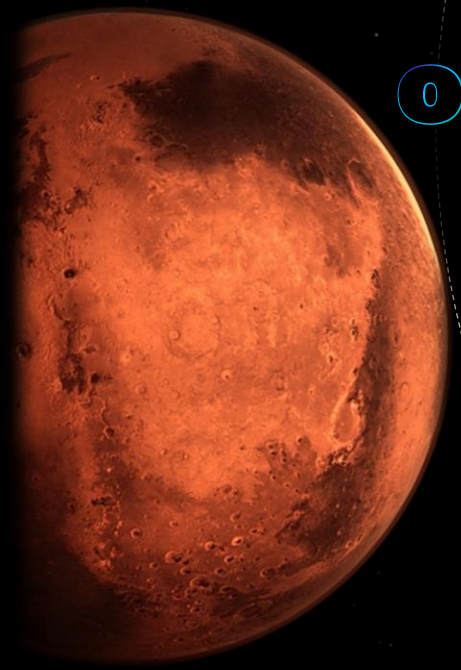
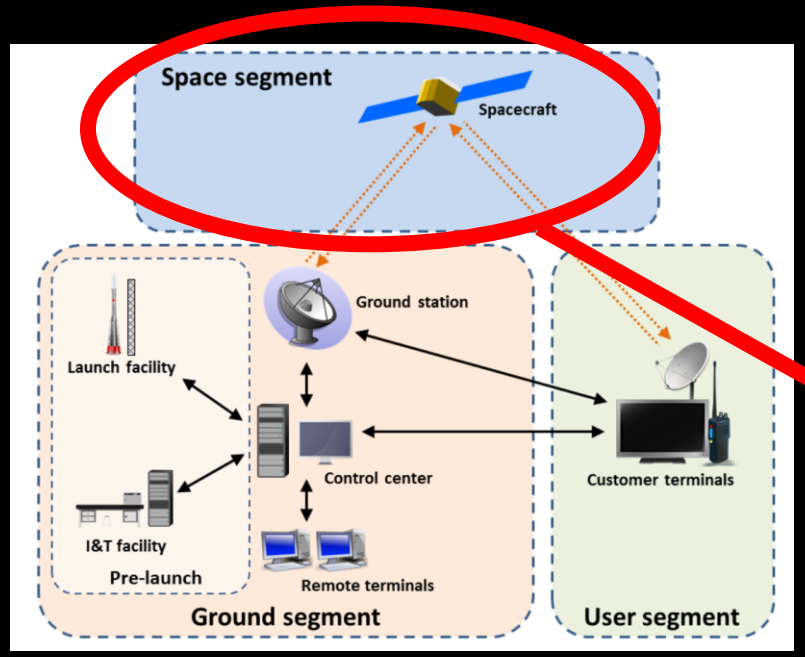


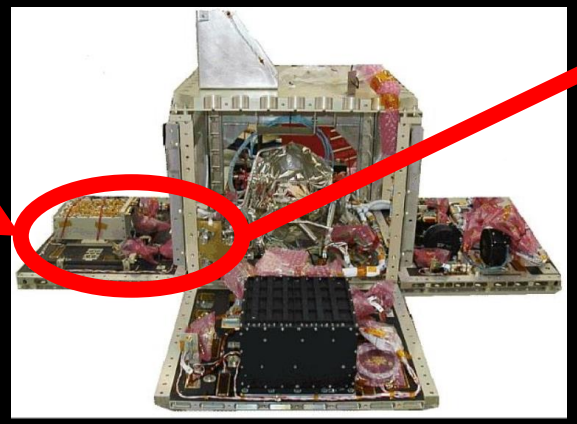
source mars © NASA/JPL Caltech, 2020

EMBEDDED SYSTEM

Functioning as part of a larger device rather than as an independent unit or system



Space system



Myriade Platform (OBC)

Myriade OBC CPU board

Section DTN/TVO/ET

- Data handling
- Cryptography
- Digital equipment
- **FPGA-SOC**

source Merriam webster dictionary
source wikipedia : https://fr.wikipedia.org/wiki/Segment_sol#/media/Fichier:Ground_segment-fr.png
source CNES (Myriade)
IA generated with prompt: « système spatial terre fusée satellite »

- *DTN : Direction Technique et Numérique (Marie-Anne Clair)*
- *TVO : Sous Direction Techniques Véhicules Orbitaux (Christophe Laporte)*
- *ET : Service Electronique numérique et Traitements bord (Roland Laulheret)*

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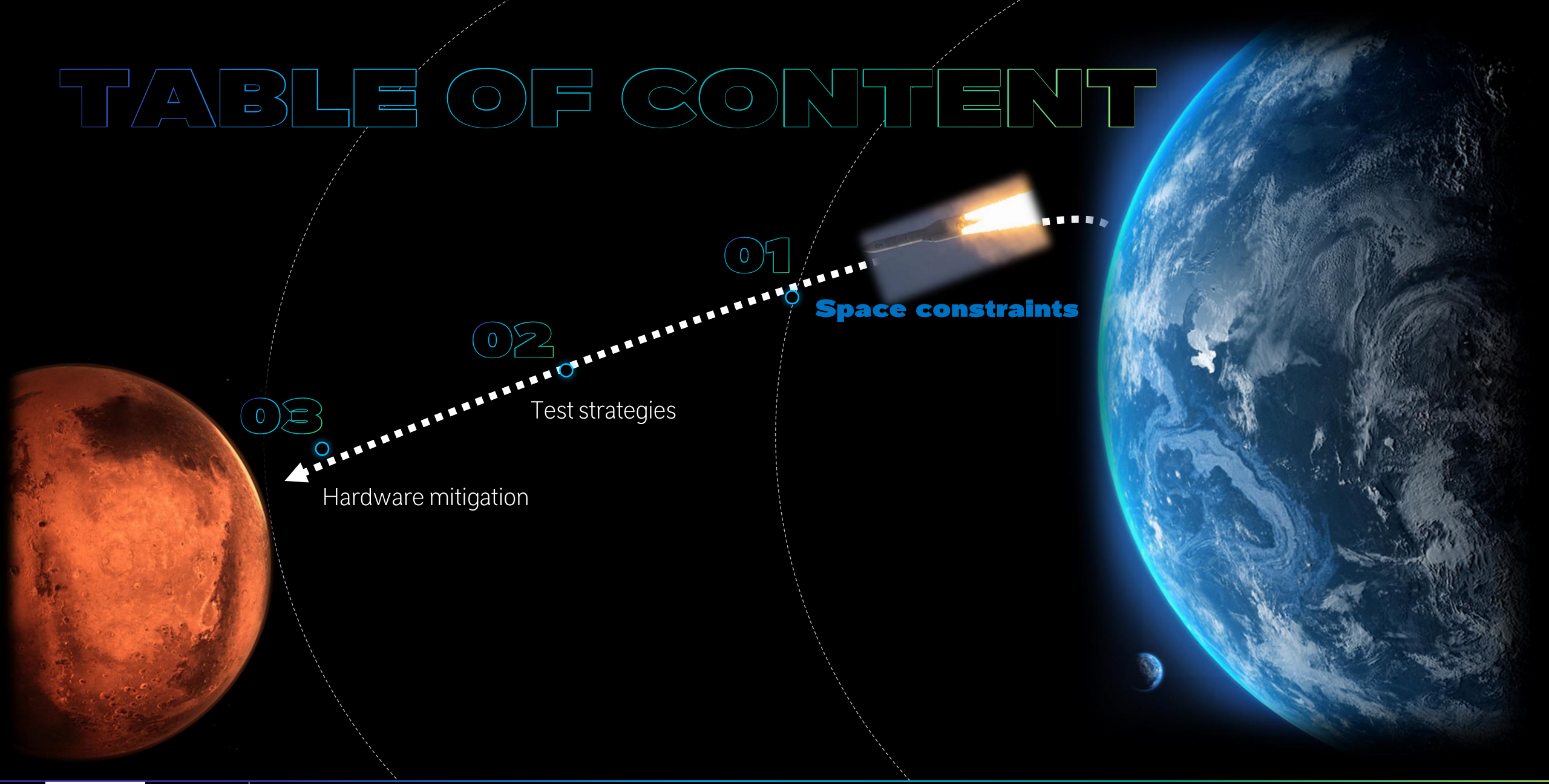


EMBEDDED CONSTRAINTS : MISSION

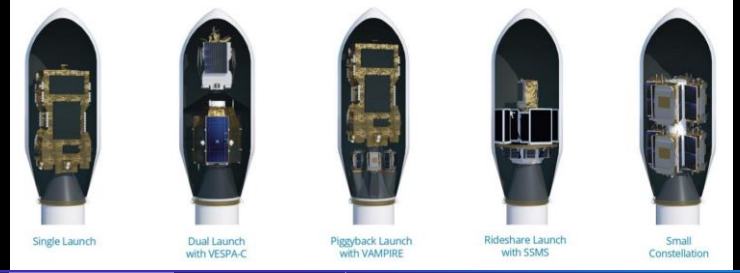
Money

Weight /Size
Launch cost

Size
Launch opportunity
Piggyback or Main satellite

Power
Battery +Solar panel size

Product assurance



Argos

Application

Performance
SNR, Resolution, Erlang..

Availability
Down time due to environment

Space destination
Orbit, planet...

Duration

Mission duration

Satellite development duration
Time to market
“Time to science”

source Ariane espace Vega C ,
CNES photothèque
credit : https://defence-industry-space.ec.europa.eu
credit : https://www.argos-system.org

Go further with tech in space : Advanced (2026) or Essentials (2027) : https://techinspace.fr/

EMBEDDED CONSTRAINTS : ENVIRONMENT

Thermal

Cycling
From -157°C to +121°C (ISS profile)
Outerspace -270°C

Space vacuum
No air =>
No dissipation, conduction and radiation only
outgazing

Temperature gradient

Mechanical

Shock
Launcher separation

Vibration
Launch

Maintenance

Reparation/Investigation
No physical access
Limited "deep-inspection"

Radiation

SEU
bitflips

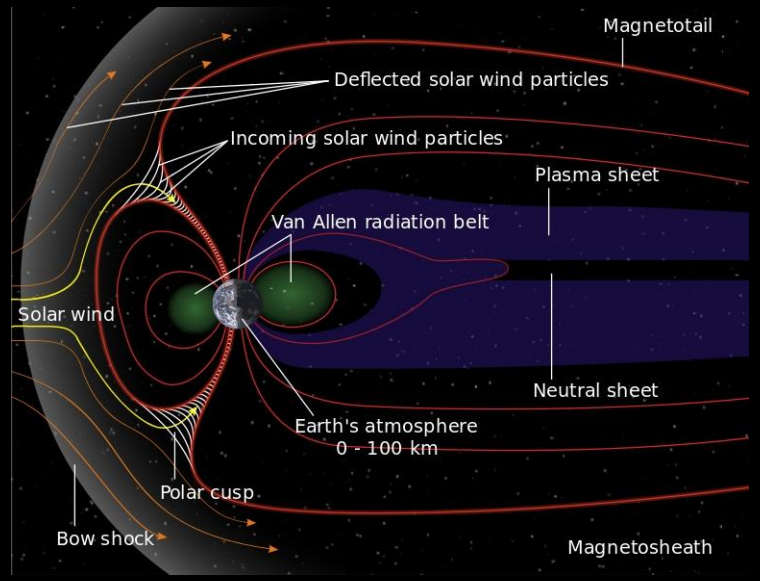
TID
Performance change

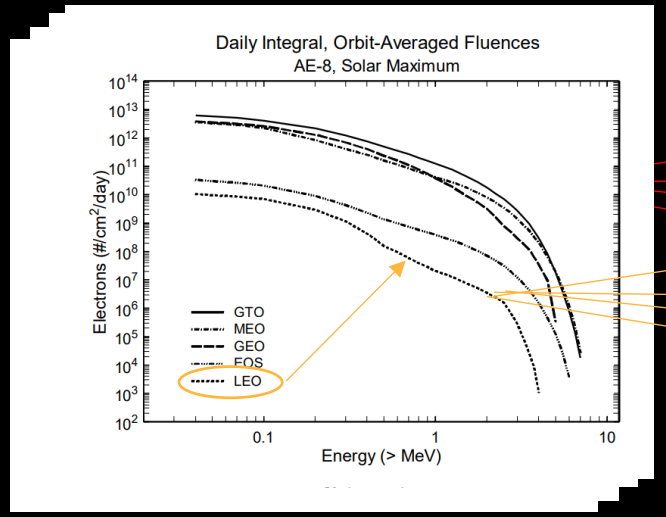
Latchup
Power shortcut

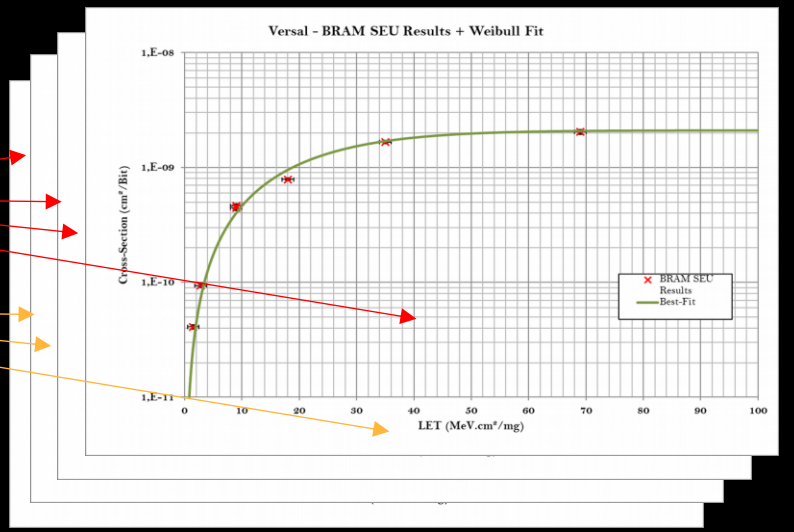
RADIATION : WHERE PROBABILITY MATTERS

- Radiation impact is based on particle hit probability
  - Occurring hazard depends on: **Orbit** (particles distribution) AND **Component sensitivity** (device cross Section)

- Radiation origin (energy keV <-> GeV) :
  - Galactic cosmic rays (ions)
  - Solar particle (protons, electrons, ions)
  - Earth radiation belts (electrons, protons)





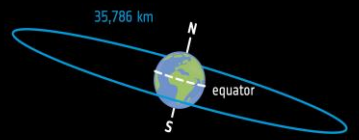


\+

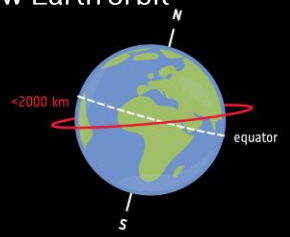
= Error Rate

- Orbits:

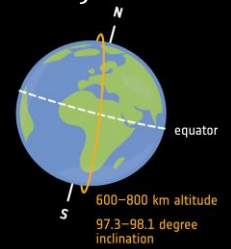
GEO
Geostationary orbit



LEO
Low Earth orbit



SSO
Polar and Sun-synchronous orbit

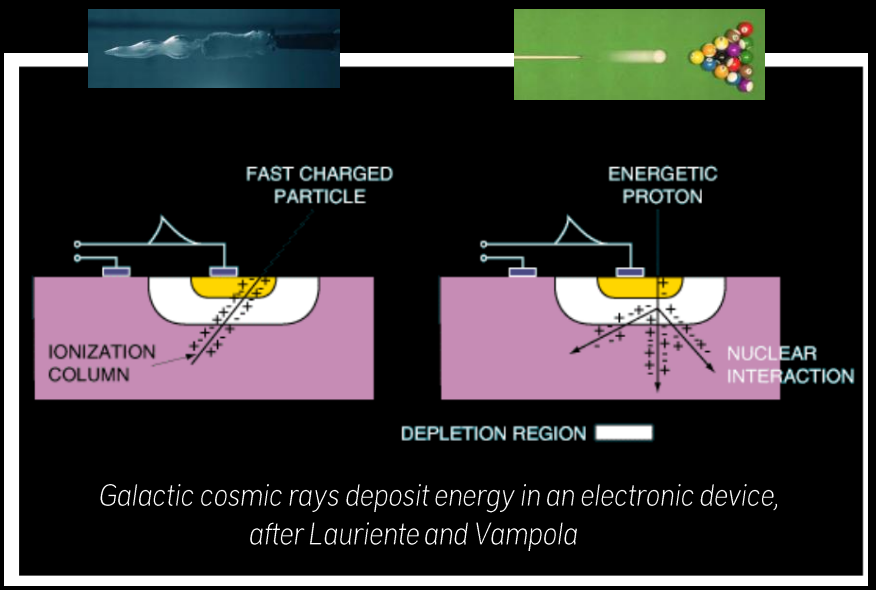


- credit :NASA rendering by Aaron Kaase credit: ESA orbits
- 1997 IEEE nuclear and Space Radiation conference : « applying computer Simulation Tools to Radiation Effect problems »: Janet barth ,GFSC :https://radhome.gsfc.nasa.gov/radhome/papers/sc_nsrec97.pdf
- Radecs 2023: Heavy-ion and proton Single Event Effect characterization of 7nm FinFET AMD VersalTM | Arnaud Dufour, Florent Manni, François Pierron, David Dangla, Françoise Bezerra, Julien Mekki1, Pierre Maillard
- logiciel Omere (Trad) : https://www.trad.fr/spatial/logiciel-omere/

RADIATION IMPACT

- Multiple impacts:
  - Component destruction (Latchup)
  - Bitflip (Single Event Upset SEU)
  - Single Event Functional Interrupt (SEFI)
  - Parametric change (Total ionizing Dose TID)
  - ….
  - ➢ Loss of availability or performance (system level)

- Latchup : " high current flows and if the power supply is maintained, the device can be destroyed by thermal effect."
- SEU "An SEU is a single bit flip, i.e. the change of state of a storage element, such as flip-flops, latches or SRAM cells"
- TID " Induced by the transfer of ionising energy from the radiation exposure, which thermalized in the creation of electron-hole pairs in the component material. "



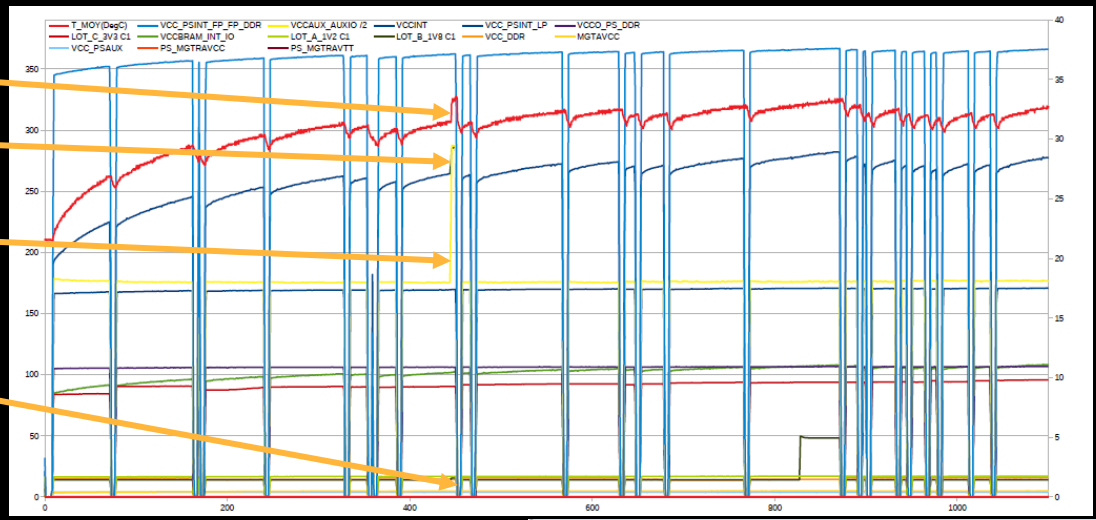
Galactic cosmic rays deposit energy in an electronic device, after Lauriente and Vampola

2. T° increase

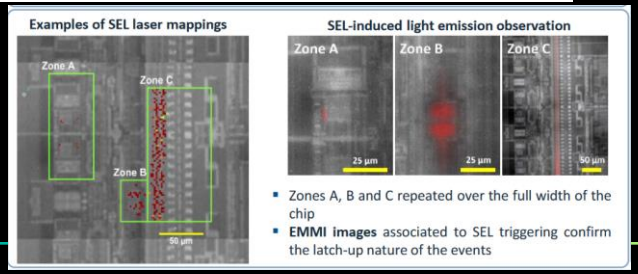
3. VCCint current increase

1. Latchup on VCCaux

4. Delatch



```
324524  "09/10/2016 02:52:23",[P7];DT7;10709185749; reg ;140841;7434;LF
324525  CR
324526  "09/10/2016 02:52:29",[P7];ÄÔ7;10714874215; òeç ;140904;7434;LF
324527  CR
324528  "09/10/2016 02:52:43",[P7];ÄT7;10729172909; reg ;141072;7434;LF
324529  CR
324530  "09/10/2016 02:52:52",[P7];DT7;10738656250; reg ;141177;7434;LF
```



source : ECSS handbook mitigation ECSS-E-HB-20-40A (11October2023).pdf
source : RADEF test for versal and Zynq ultrascale+ MPSOC (CNES)
source : Rapport SEE Zynq ultrascale+ MPSOC (RR1772AEd1,CNES/Bibench)

CNES journée des jeunes chercheurs:
"Analysis of the Single-Event Latch-up Cross Section of a 16nm FinFET System-on-Chip using Backside Single-Photon Absorption Laser Testing and Correlation with Heavy Ion Data ng and Correlation with Heavy Ion Data"
M. Fongral1, V. Pouget1, F. Saigne1, M. Ruffenach2, J. Carron2, F. Malou2, J. Mekki

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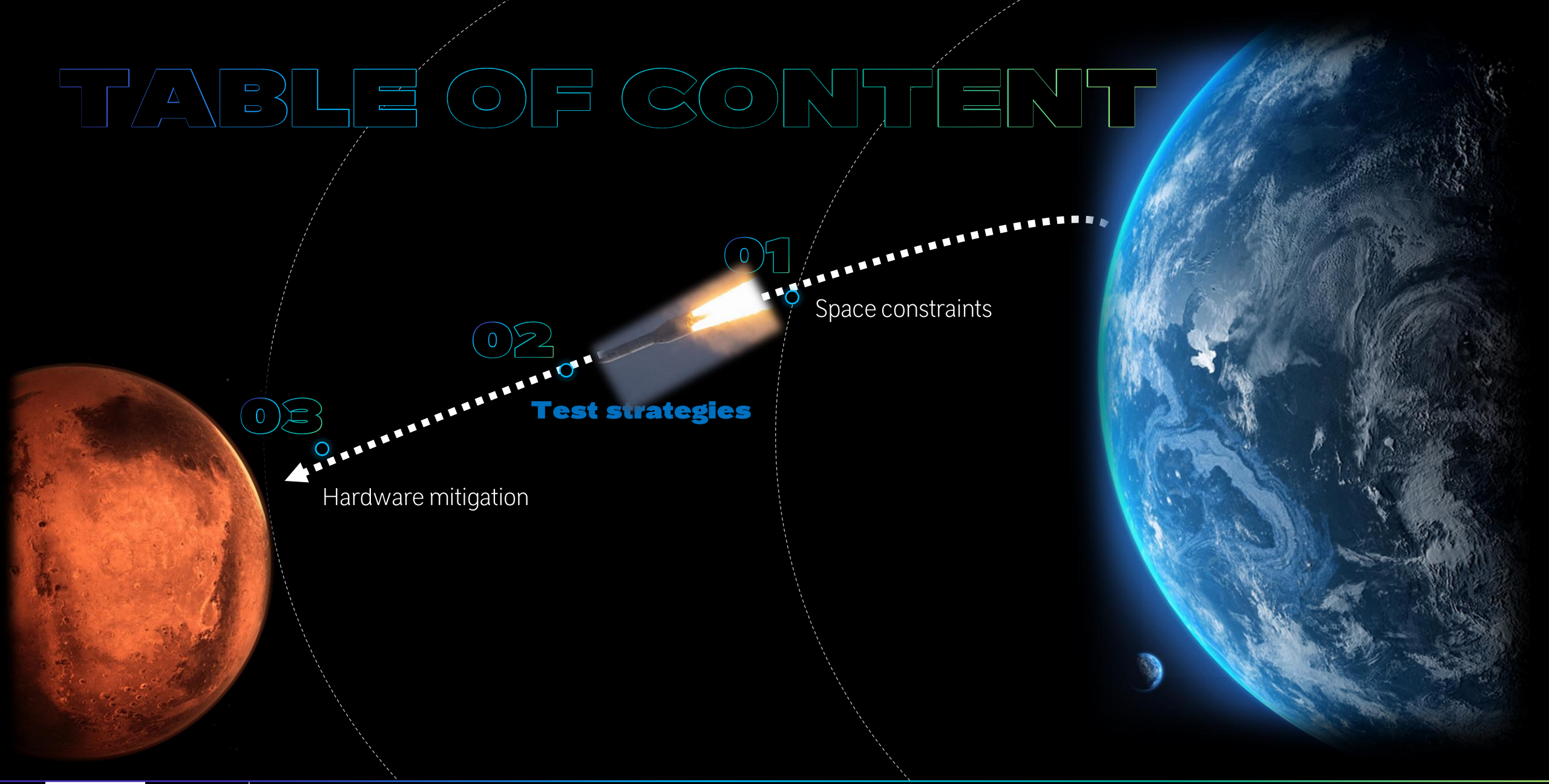
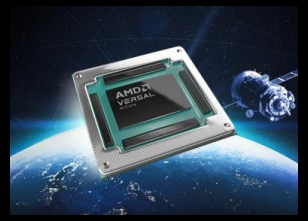


COMPONENT SELECTION

	Performance	Price	quality
RadHard	+	++(+)	++(+)
RadTol	++(*)	++	++
COTS	+++	+	+

- RadHard (Radiation Hardened)
  - Built for radiation (specific silicon process/PDK or IP libraries)
  - Radiation guaranteed by datasheet
  - Space quality certified ESCC or QML
  - Silicon die controlled tracability



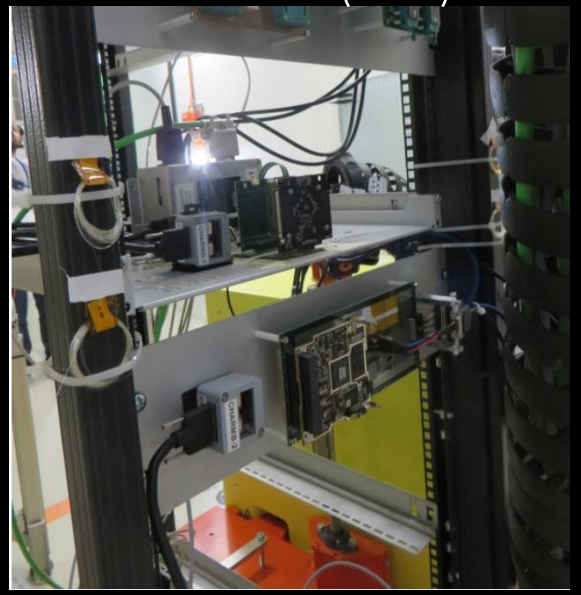
- RadTol (Radiation Tolerant)
  - « Everyday component » sold for space use
  - Most of the time COTS rebranded for space after dedicated tests
  - Radiation data and qualification variable

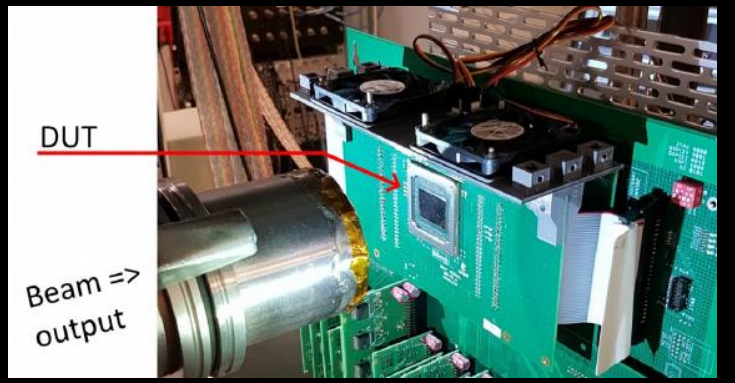
- COTS (Commercial Off-The-Shelf)
  - Generic application component (built for other market than space)
  - Need custom/adapted quality « upgrade »

RADIATION TEST STRATEGIES

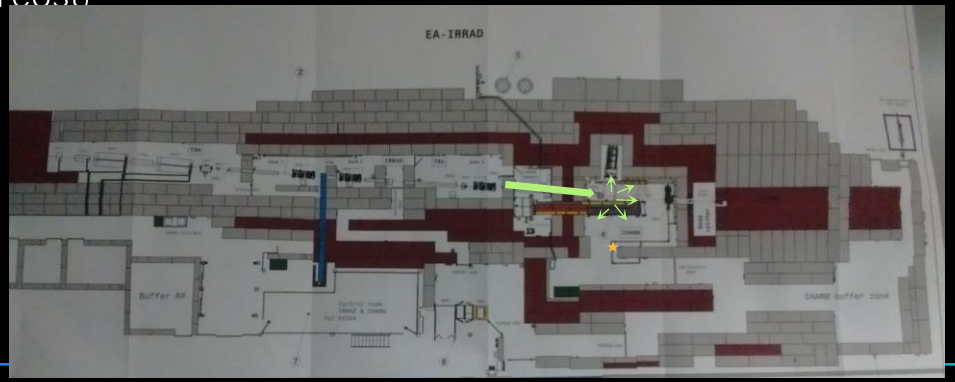
- **Component level**
  - Procure COTS lot
  - Test them against radiation events (latchup , SEU..)
  - => Establish detailed cross section
- **Equipment level**
  - Procure equipment
  - Test it in high energy facility
    - Establish failure mode and recovery ,
    - TID
- **No test**
  - « Technological opportunism » (time-to-market versus mission global cost)
  - Marketing objective
  - Use of RadHard components

Zynq based CNES OBC Ninano tested at CHARM (CERN)





Versal component test set



SpaceX/Tesla ads

Carte test radiation Versal: BIBENCH (Jyväskylä)
Roue à réaction : HYPERION TECHNOLOGIES HT-RW210
TESLA/SPACEX
H. Quinn, "Challenges in Testing Complex Systems," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 2, pp. 766-786, April 2014,

COMPONENT FLOW CHART EXAMPLE

1. Assess requirements for the equipment
   - choose between equipment test or component
2. Identification of component technology
   - Radhard => no test to be performed
   - Radtol => do error rate calculus based on vendor data
   - COTS => Assess project scope (budget, availability, performances)
3. COTS is selected AND tests are needed
   1. Perform Latchup test => can be used in space
   2. Perform SEU tests => error rate estimation
   3. Perfom TID tests => confirm mission duration
4. Assess mission performances and availability using calculus
   1. Calculate worst case error rate => acceptable?
   2. Assess mission performance and availability
   3. Refine your error rate calculus hypothesis => acceptable? (memory size, essential bits, data path control path..)
   4. Assess mission performance and availability
   5. Add mitigation to your error rate calculation => acceptable?
   6. Assess mission performance and availability

sample preparation

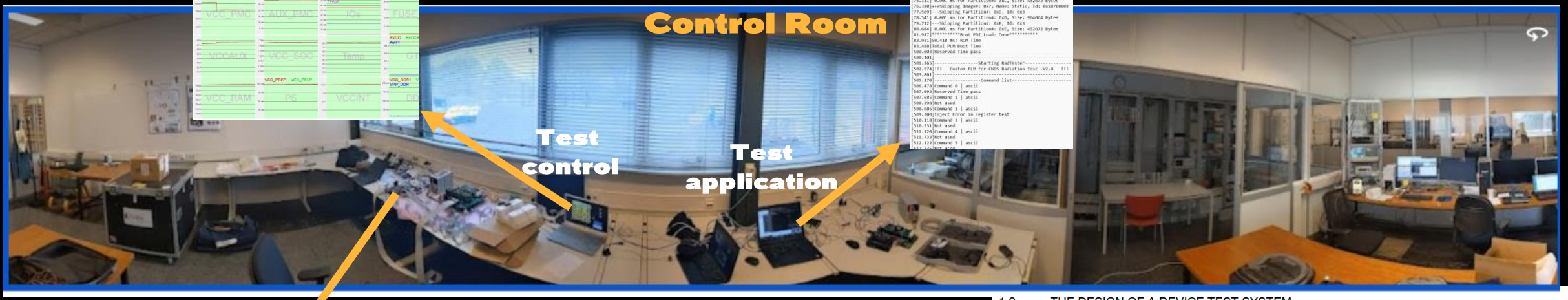
Nom Complet	Quoi
VREFP	PL System Monitor externally supplied reference voltage
VCCINT	PL internal supply voltage
VMGTAVCC	Analog supply voltage for the GTH or GTY transceiver
VPS_MGTRAVCC	PS-GTR supply voltage
VCC_PSINTFP	PS full-power domain supply voltage
VCC_PSINTFP_DDR	PS DDR controller and PHY supply voltage
VCC_PSINTLP	PS low-power domain supply voltage
VCCBRAM	Block RAM supply voltage
VCCINT_IO	PL internal supply voltage for the I/O banks
VMGTAVTT	Analog supply voltage for the GTH or GTY Transmitter and receiver termination circuits
VMGTAVTTRCAL	Analog supply voltage for the resistor
VCC_INSIDE_1V2	Alim 1V2 pour la carte inside (COM => ZU)
VCC_PSPLL	PS PLL supply voltage
VCCO_64	Supply voltage for HP I/O bank 64
VCCO_65	Supply voltage for HP I/O bank 65
VCCO_66	Supply voltage for HP I/O bank 66
VCC_DDR	Alim des mémoires DDR3 sur la carte DUT
VCCO_PSDDR	PS DDR I/O supply voltage
VCC_PSBATT	PS battery-backed RAM and battery-backed Real-time clock (RTC) supply voltage
VMGTVCCAUX	Auxiliary analog QPLL voltage supply for the transceivers
VCC_INSIDE_1V8	Alim 1V8 pour la carte inside (COM => ZU)
VCC_PSADC	PS SYSMON ADC supply voltage
VCC_PSDDR_PLL	PS DDR PLL supply voltage
VCCADC	PL System Monitor supply
VCCO_67	Supply voltage for HP I/O bank 67
VCCO_68	Supply voltage for HP I/O bank 68
VCCO_69	Supply voltage for HP I/O bank 69
VCCO_70	Supply voltage for HP I/O bank 70
VCCO_71	Supply voltage for HP I/O bank 71
VCCO_72	Supply voltage for HP I/O bank 72
VCCO_73	Supply voltage for HP I/O bank 73
VCCO_74	Supply voltage for HP I/O bank 74
VPS_MGTRAVTT	PS-GTR termination voltage
VCC_PSAUX	PS auxiliary supply voltage
VCCAUX	Auxiliary supply voltage
VCCAUX_IO	Auxiliary I/O supply voltage
VCC_INSIDE_3V3	Alim 3V3 pour la carte inside (COM => ZU)
VCC_QSPI	Alim de la mémoire QSPI sur la carte DUT
VCCO_90	Supply voltage for HD I/O bank 90
VCCO_91	Supply voltage for HD I/O bank 91
VCCO_93	Supply voltage for HD I/O bank 93
VCCO_PSIO_500	PS I/O supply bank 500
VCCO_PSIO_501	PS I/O supply bank 501
VCCO_PSIO_502	PS I/O supply bank 502
VCCO_PSIO_503	PS I/O supply bank 503 (config)

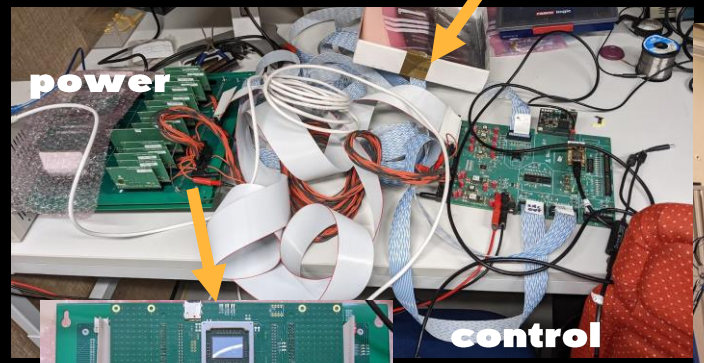
UltraCOM (CNES)

ZU+ latchup monitoring

4.' Assess mission performances and availability using test as you fly
   1. Prepare component irradiation with representative HW/SW
   2. Do irradiation test
   3. Extrapolate mission availability and performances

SEU TEST VERSAL EXAMPLE - PARTREC (NETHERLAND)





1.2 THE DESIGN OF A DEVICE TEST SYSTEM

The Test System is device specific; however, there are a number of general principles which apply. The basic operations required of a Test System are:

(a) Device initialisation and function test.
(b) Device operation, dynamic or static, during exposure.
(c) Device latch-up protection, logging and re-initialisation.
(d) Detection of all types of errors or failures, logging and rewriting of an affected part of the tested device, software and hardware re-initialisation, and power control.
(e) Measurement and logging of the "duty cycle" (fraction of time the device is active and vulnerable to upset compared with the test time).
(f) Logging of test time, count rates, fluence and beam diagnostics to be attached to the test data.

The following additional features enhance test throughput and flexibility:

(a) Real time data processing, storage and retrieval.
(b) Reconfiguration under software control, particularly for the testing of different memory organisations.
(c) High operating speed and duty factor.
(d) Real time device under test data display.
(e) Data reduction while tests are in progress to allow test conditions to be modified depending on results achieved.

Do not underestimate post-processing time !

- source Single Event Effects Test Method and Guidelines – ESCIES : https://escies.org/download/specdraftapppub?id=3095

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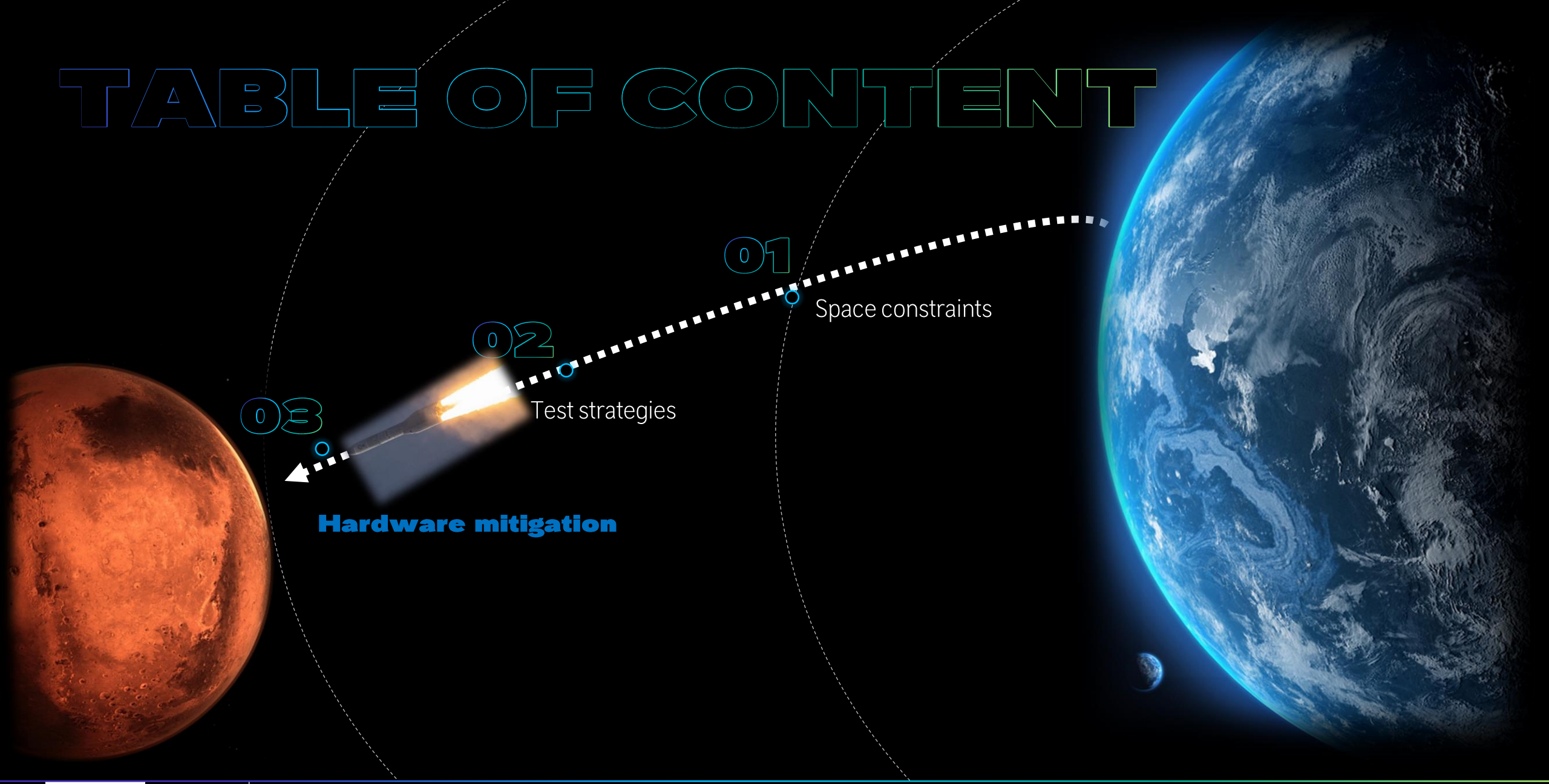


source mars © NASA/JPL Caltech, 2020

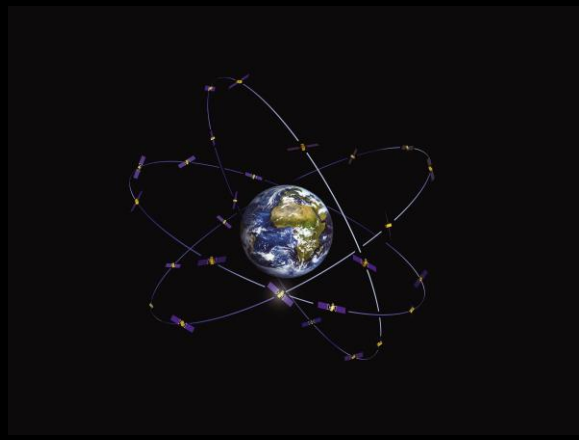
MITIGATION : MANY POSSIBILITIES

Project development

Beginning

In flight

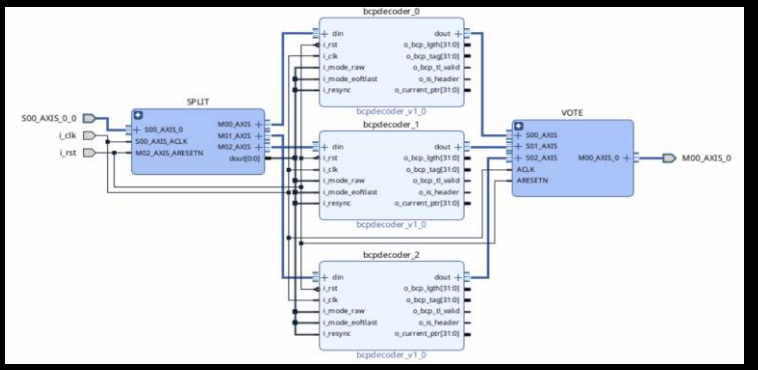
- **System level :**
  - Satellite « hot » redundancy (constellation)
  - Satellite « cold redundancy » (spare satellite)
  - Periodic ON/OFF,
  - Decrease revisit period
- **Equipment level :**
  - Cold or hot redundancy
  - Duplication/Triplication + vote
- **Board level:**
  - Radhard components
  - Watchdog, delatch, duplex/triplex…
  - Power it off (QSPI)
- **Internal component level (µP, FPGA, SOC)**
  - Error code for BRAM
  - Scrubbing
  - Hypervisor
  - Don’t use the function (cache, peripheral..)



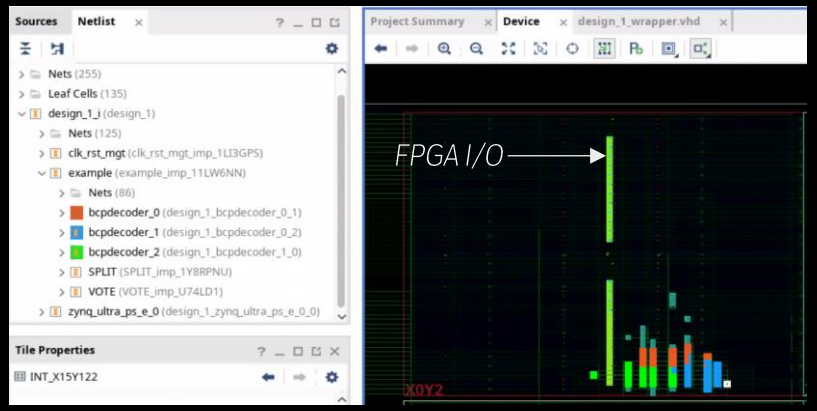
DTN/TVO/ET/2022-07611 : 08/06/2022 : Radiation Mitigation Guideline for Xilinx Devices
ECSS-Q-HB-60-02A : Techniques for radiation effects mitigation in ASICs and FPGAs handbook

MITIGATION 1 : KEEP IT SIMPLE

- Example of TMR (Triple Modular redundancy) in an SRAM based COTS FPGA : Xilinx
  - Did I consider synthesis optimization (replication /sharing ...) ?
    - ➢ Perform log analysis and VHDL pragma use
  - Did I consider configuration user bit SEU ?
    - Perform floorplanning
  - Did I consider configuration user bit SEU ?
    - Perform isolation flow
  - Did I consider clock SET?
    - Perform different clock insertion in each module
  - Did I consider I/O SET?
    - Perform I/O splitting for each module



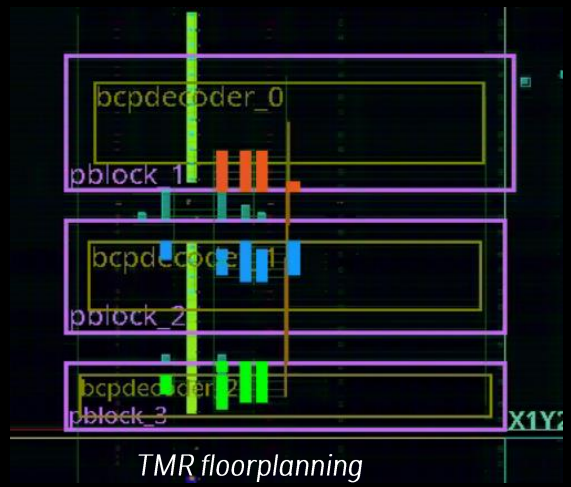
initial floorplanning



➢ Simple bitstream scrubbing with associated ON/OFF might be more efficient?

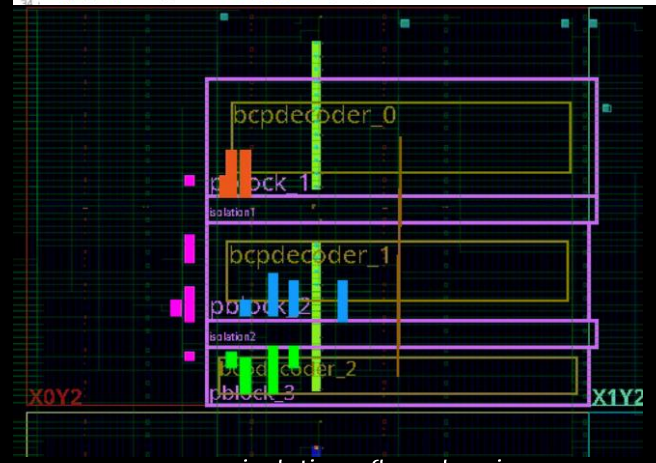
```
292 # ----------------------------------------------------------------------------------------------------
293 # ------------------------------Bitstream generation constraints --------------------------------
294 #http://www.xilinx.com/support/answers/51148.html
295
296 #activate the scrubbing of the FPGA
297 set_property bitstream.general.post_crc_en yes [current_design]
298
299 #select scrubbing post crc frequency (not used for the moment)
300 #set_property bitstream.general.post_crc_freq 50 [current_design]
301
302 #error are reported through pulse in init_b (default mode)
303 set_property bitstream.general.post_crc_init_flag Enable [current_design]
304
305 #pre compute frame ECC  . The CRC is not calculed at boot but precalculed inside bitstream (avoid init problem)
306 set_property bitstream.general.post_crc_sel 1 [current_design]
307
308 #select action in case of error : correct and continue
309 set_property bitstream.general.post_crc_keep yes [current_design]
310 set_property bitstream.general.post_crc_correct yes [current_design]
311
```

ex : Xilinx Zynq scrubbing activation through constraint



TMR floorplanning

```
23 :
24 : create_pblock pblock_3
25 : add_cells_to_pblock [get_pblocks pblock_3] [get_cells -quiet [list design_1_i/example/bcpdecoder_2]]
26 : resize_pblock [get_pblocks pblock_3] -add {SLICE_X9Y120:SLICE_X28Y128}
27 : resize_pblock [get_pblocks pblock_3] -add {DSP48E2_X1Y48:DSP48E2_X2Y49}
28 : resize_pblock [get_pblocks pblock_3] -add {RAMB18_X1Y48:RAMB18_X2Y49}
29 : resize_pblock [get_pblocks pblock_3] -add {RAMB36_X1Y24:RAMB36_X2Y24}
30 : set_property EXCLUDE_PLACEMENT TRUE  [get_pblocks pblock_3]
31 : # not set per default
32 : set_property IS_SOFT  false [get_pblocks pblock_3]
33 : set_property CONTAIN_ROUTING true [get_pblocks pblock_3]
```



« isolation » floorplanning

MITIGATION 2: NOT TESTED = NOT WORKING

Block RAM and FIFO ECC Port Descriptions

Table 1-31 lists and describes the block RAM and FIFO ECC-related I/O port names.

Table 1-31: **RAMB36E2 and FIFO32E2 ECC Port Names and Descriptions**

Port Name	Signal Description
INJECTSBERR	Injects a single-bit error if ECC is used. Creates a single-bit error at a particular block RAM bit location when asserted during write. The block RAM ECC logic corrects this error when this location is read back. The error is created in bit DIN[30].
INJECTDBERR	Injects a double-bit error if ECC is used. Creates a double-bit error at two particular block RAM bit locations when asserted during write. The block RAM ECC logic flags a double-bit error when this location is read back. When both INJECTSBERR and INJECTDBERR signals are simultaneously asserted, a double-bit error is injected. The errors are created in bits DIN[30] and DIN[62].
ECCPARITY[7:0]	ECC encoder output bus for ECC used in encode-only mode. This output cannot be cascaded.
SBERR	ECC single-bit error output status. See also the dedicated cascade pins in this table when using the block RAM and FIFO in ECC cascade mode.(1)
DBERR	ECC double-bit error output status. See also the dedicated cascade pins in this table when using the block RAM and FIFO in ECC cascade mode.(1)
RDADDRECC[8:0]	ECC read address. Address pointer to the data currently read out. The data and corresponding address are available in the same cycle. This output is not supported in the FIFO and cannot be cascaded.
CASINSBITERR	ECC single-bit error input in cascade mode. Cascade SBERR error bit status from the previous block RAM/FIFO.
CASOUTSBITERR	ECC single-bit error output in cascade mode. Cascade SBERR error bit status to the next block RAM/FIFO.
CASINDBITERR	ECC double-bit error input in cascade mode. Cascade DBERR error bit status from the previous block RAM/FIFO.
CASOUTDBITERR	ECC double-bit error output in cascade mode. Cascade DBERR error bit status to the next block RAM/FIFO.

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Chapter 1: **Block RAM Resources**

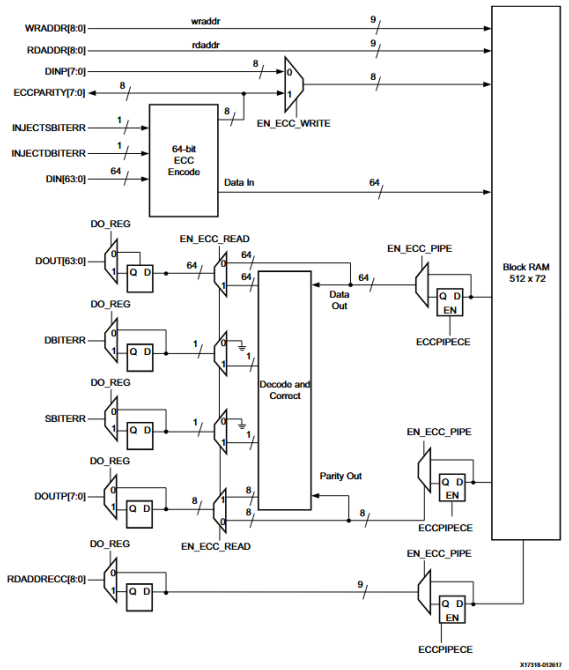

Figure 1-32: **Top-Level View of Block RAM ECC**

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Chapter 1: **Block RAM Resources**

Built-in Error Correction

Overview

The RAMB36E2 in simple dual-port mode can be configured as a single 512 x 64 RAM with built-in Hamming code error correction using the extra eight bits in the 72-bit wide RAM. This operation is transparent.

No need for custom made ECC for RAM

The ECC configuration option is available with a 36 Kb block RAM (RAMB36E2) in simple dual-port mode 72-bit width (64/8) (SDP) or a 36 Kb FIFO (FIFO36E2) in 72-bit width. Both read and write width must be 72 bits. The RAMB36E2 has the capability to inject errors. The RAMB36E2 has the ability to read back the address where the current data read out is stored. This feature better supports repairing a bit error or invalidating the content of that address for future access. The FIFO36E2 supports standard ECC mode with both the WRITE_WIDTH and READ_WIDTH set to 72 and has error-injection capability. FIFO36E2 does not output the address location being read.

Be careful there are some additionnal constraints

During each read operation, 72 bits of data (64 bits of data and 8 bits of parity) are read from the memory and fed into the ECC decoder. The ECC decoder generates two status outputs (SBITERR and DBITERR) that are used to indicate the three possible read results: No error, single-bit error corrected, and double-bit error detected. In the standard ECC mode, the read operation does not correct the error in the memory array, it only presents corrected data on DOUT. To improve F_{MAX}, optional registers controlled by the DO_REG attribute are available for data output (DOUT), SBITERR, and DBITERR. This is similar to the optional registers in the block RAM. For further F_{MAX} improvements, an additional ECC pipeline stage is available.

Still scrubbing is needed

- Xilinx BRAM includes Hamming ECC
  - Testing the feature was identified as to complicated on ground
  - This is a Xilinx built-in feature so it is working!
- No SEU reported in flight
  - ECC not functional ?
  - Wrong logging mechanism ?

- source Ultrascale architecture memory resources user guide (UG573) Xilinx

MITIGATION 3: TEST REPRESENTATIVE

ANNEX 7: FAILURE ANALYSIS WATCHOG PIC 07/10/2016 13:48 EVENT

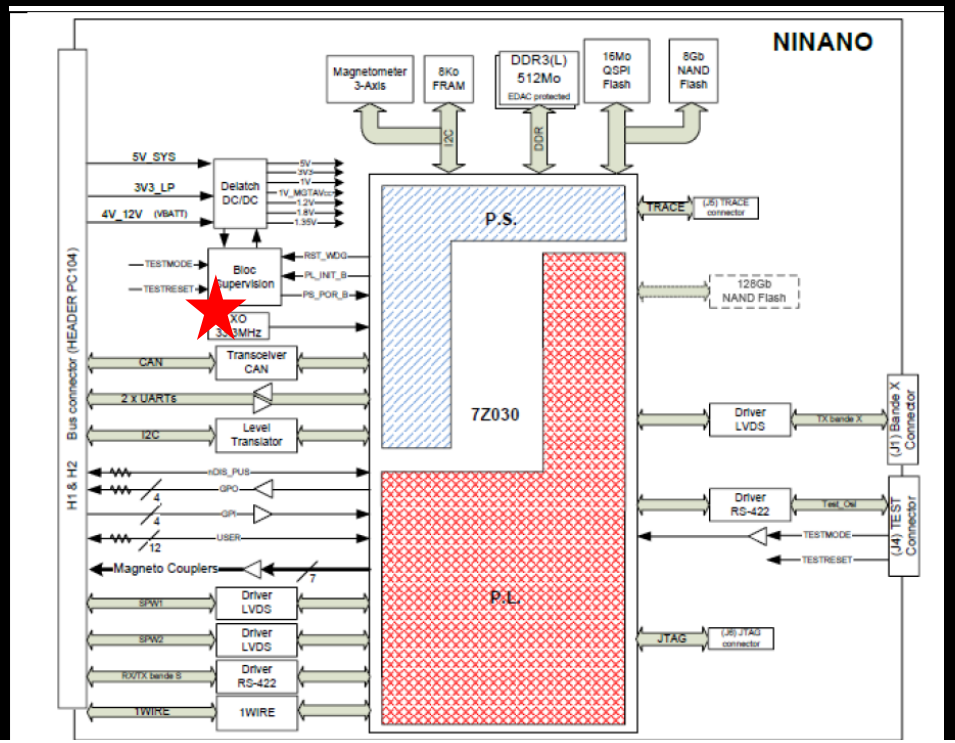
At 13h48:19, the system shows a particular event. The log below mix Pic log and Xtratum logs to get an overview of the problem.

```
07/10/2016 13:27:26          #  128  14  1  6  1  2
07/10/2016 13:48:10,[P6],I;Err Bram at @ 0x83c1eefc - Got 0x83c1eafc - Exp 0x83c1eefc
07/10/2016 13:48:10,[P0];EP0;1244290927; Watchdog Pic refresh;
07/10/2016 13:48:10,[P0];EP0;1244390928; Watchdog Pic refresh;
07/10/2016 13:48:10,[P6];DT8;1244463959; ddr ;1770;0;
07/10/2016 13:48:10,[P0];EP0;1244490927; Watchdog Pic refresh;
07/10/2016 13:48:10,[P0];EP0;1244590927; Watchdog Pic refresh;
07/10/2016 13:48:19      *  2  129  14  1  6  1  2          Start of error
07/10/2016 13:48:29      *  2  130  14  1  6  1  2  10
07/10/2016 13:48:38      *  2  131  14  1  6  1  2  9
07/10/2016 13:48:48      *  2  132  14  1  6  1  2  10
07/10/2016 13:48:57      *  2  133  14  1  6  1  2  9
07/10/2016 13:49:07      *  2  134  14  1  6  1  2  10
07/10/2016 13:49:17      *  2  135  14  1  6  1  2  10
07/10/2016 13:49:26      *  2  136  14  1  6  1  2  9
07/10/2016 13:49:36      *  2  137  14  1  6  1  2  10
07/10/2016 13:49:46      *  2  138  14  1  6  1  2  10
07/10/2016 13:49:55      *  2  139  14  1  6  1  2  9
07/10/2016 13:50:05      *  2  140  14  1  6  1  2  10
07/10/2016 13:50:14      *  2  141  14  1  6  1  2  9
07/10/2016 13:50:24      *  2  142  14  1  6  1  2  10
07/10/2016 13:50:34      *  2  143  14  1  6  1  2  10
07/10/2016 13:50:43      *  2  144  14  1  6  1  2  9
07/10/2016 13:50:53      *  2  145  14  1  6  1  2  10
07/10/2016 13:51:02      *  2  146  14  1  6  1  2  9
07/10/2016 13:51:12      *  2  147  14  1  6  1  2  10
07/10/2016 13:51:22      *  2  148  14  1  6  1  2  10
07/10/2016 13:51:31      *  2  149  14  1  6  1  2  9
07/10/2016 13:51:41      *  2  150  14  1  6  1  2  10
07/10/2016 13:51:51      *  2  151  14  1  6  1  2  10
07/10/2016 13:52:00      *  2  152  14  1  6  1  2  9
07/10/2016 13:52:10      *  2  153  14  1  6  1  2  10
07/10/2016 13:52:19      *  2  154  14  1  6  1  2  9
07/10/2016 13:52:29      *  2  155  14  1  6  1  2  10
07/10/2016 13:52:39      *  2  156  14  1  6  1  2  10
07/10/2016 13:52:48      *  2  157  14  1  6  1  2  9
07/10/2016 13:52:58      *  2  158  14  1  6  1  2  10
07/10/2016 13:53:07      *  2  159  14  1  6  1  2  9
07/10/2016 13:53:17      *  2  160  14  1  6  1  2  10
07/10/2016 13:53:27      *  2  161  14  1  6  1  2  10
07/10/2016 13:53:36      *  2  162  14  1  6  1  2  9
07/10/2016 13:53:44      *  2  163  14  1  6  1  2  8   Manual ON/OFF
07/10/2016 13:53:44      *  2  163  14  1  6  1  2  0   End of error
07/10/2016 13:53:52,XM Hypervisor (2.0 r4) Built Aug 26 2016 11:35:07
```

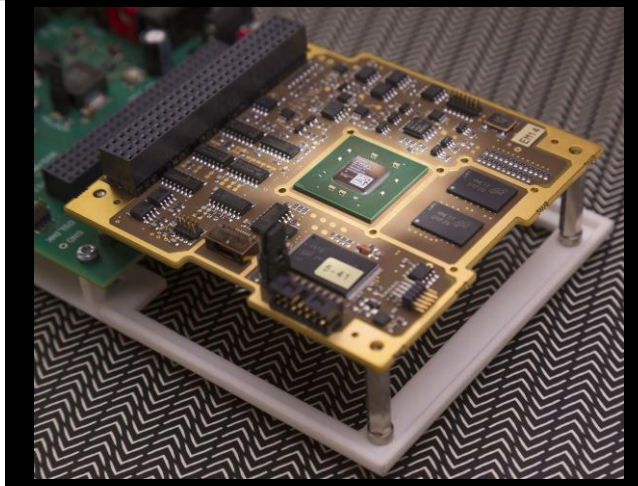
Nominal

automatic reboot by watchdog

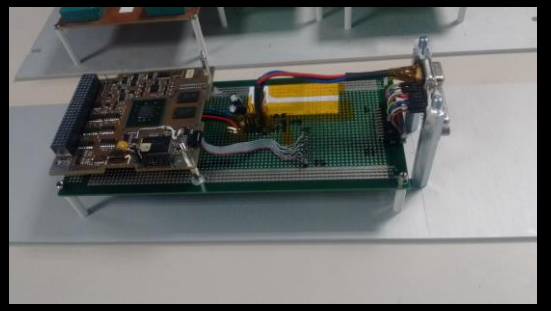
Nominal



The main hypothesis is that during the first boot, as there was an error programming the FPGA. As a Power-On-Reset is issued all registers are reset (see UG585 6- 26.5 Register Overview). So the error in the FPGA programming phase is not correctable by a simple reset but only correctable by power cycling (which is not issued in type 2 sequence in Pic Watchdog).



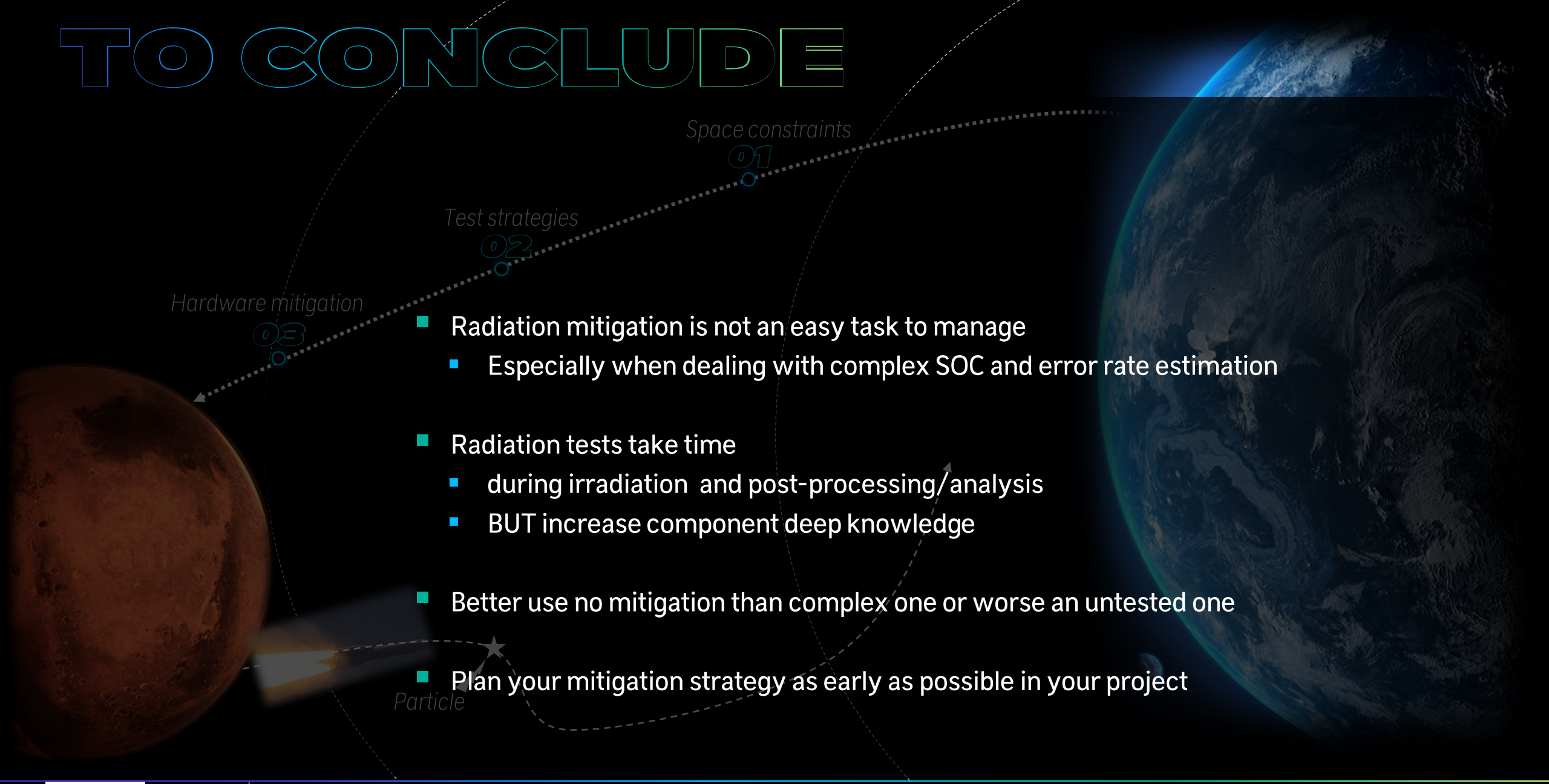
Ninano OBC



Ninano CHARM test setup

- Back to mitigation 1 : keep it simple
  - No more boot sequence monitoring : basic timing sequence implementation without feedback from FPGA
  - Afterward got rid of microcontroller and use simple RC timer instead

TO CONCLUDE



- Radiation mitigation is not an easy task to manage
  - Especially when dealing with complex SOC and error rate estimation
- Radiation tests take time
  - during irradiation and post-processing/analysis
  - BUT increase component deep knowledge
- Better use no mitigation than complex one or worse an untested one
- Plan your mitigation strategy as early as possible in your project

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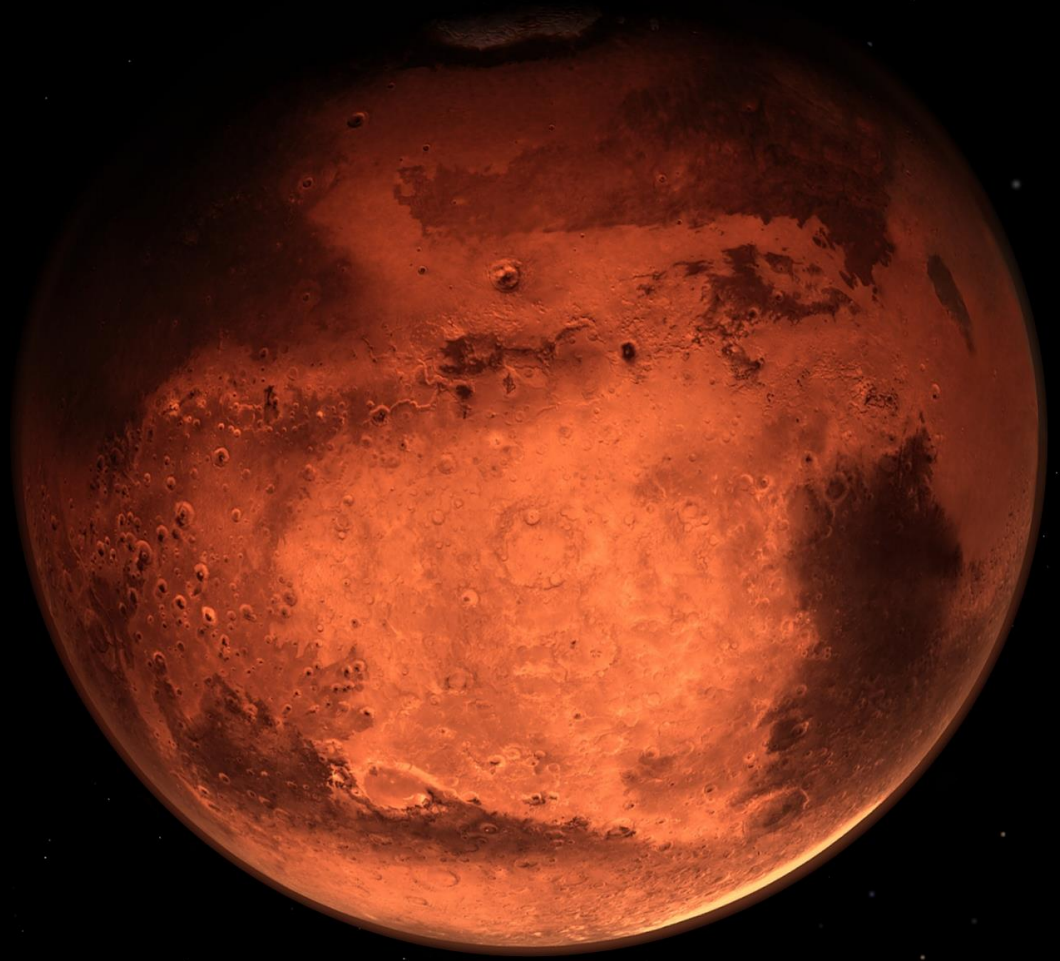
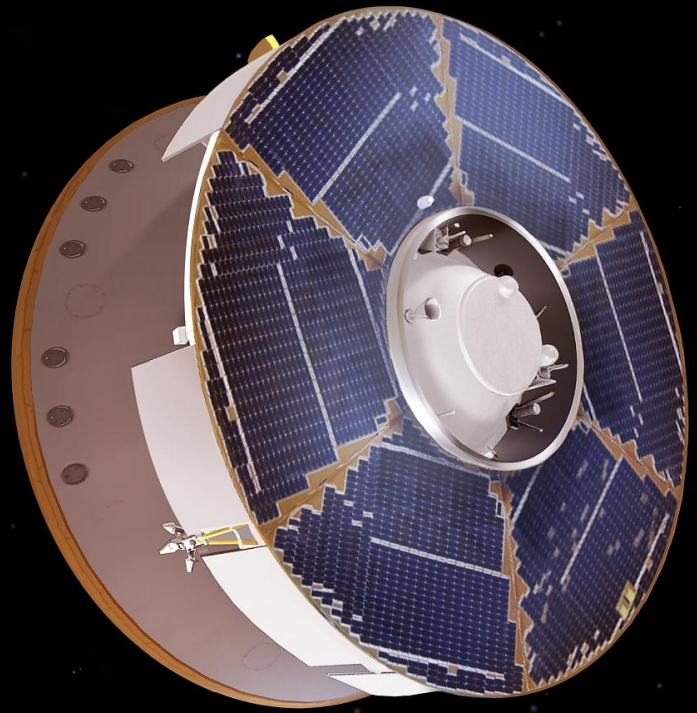
THANK YOU





ANY QUESTION?

contact : florent.manni@cnes.fr

Rover Perseverance Mars 2020.
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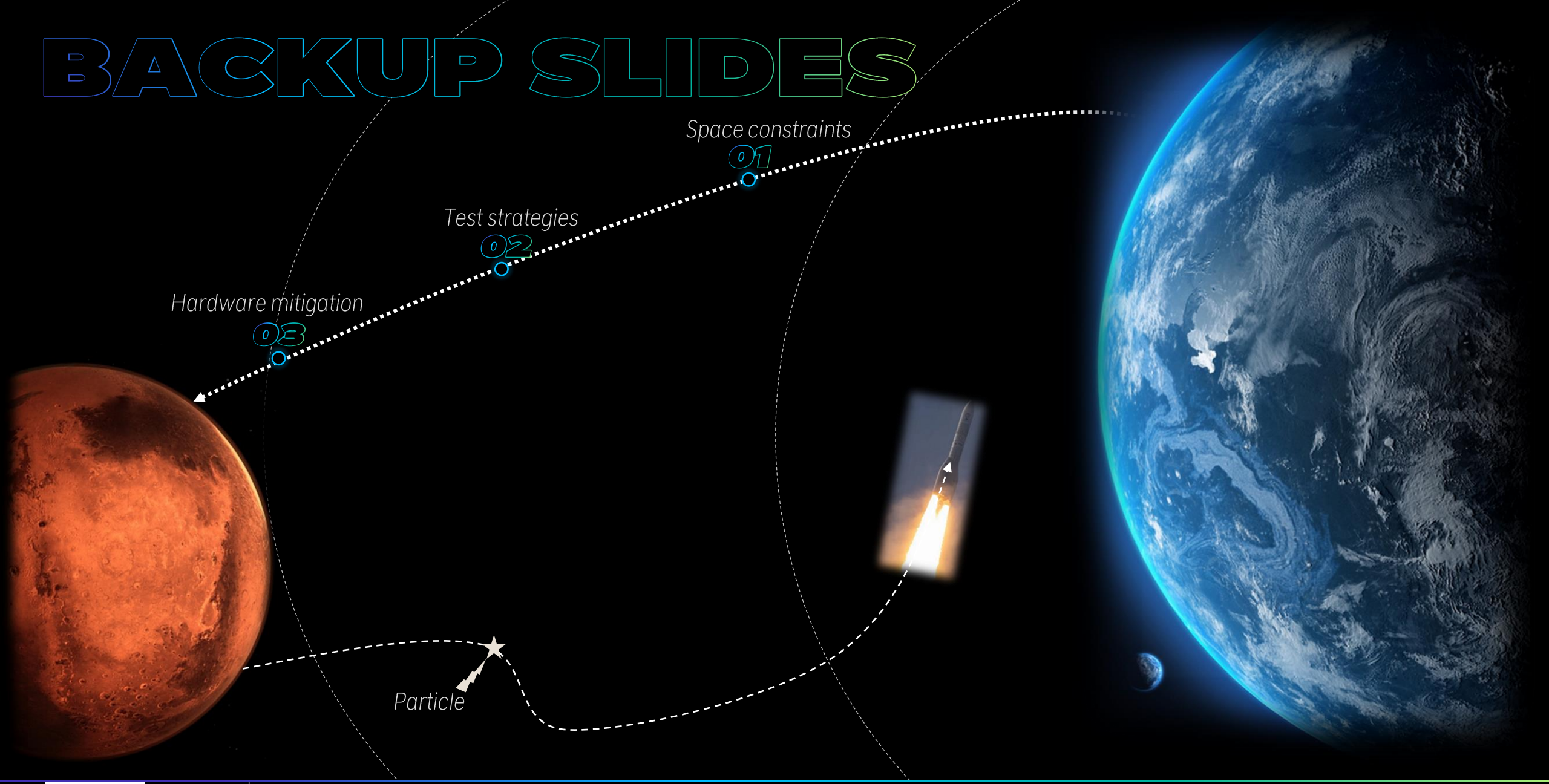
BACKUP SLIDES



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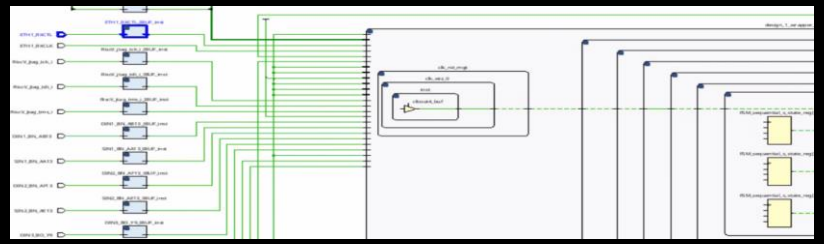
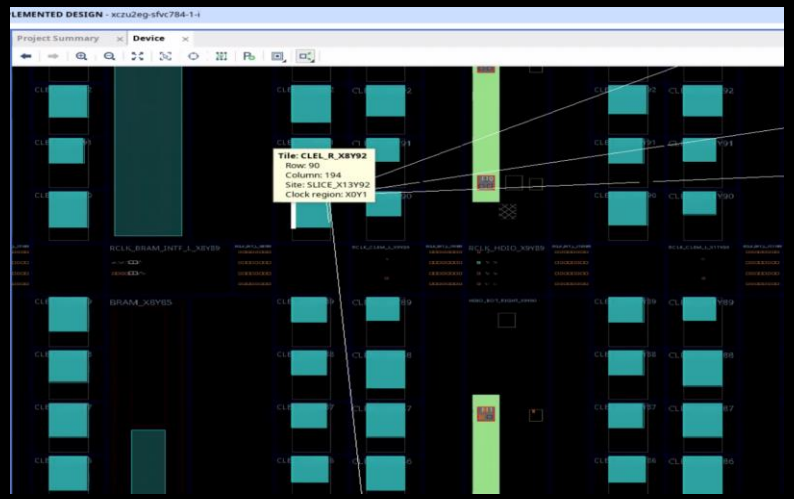
FPGA 1/2

Field programmable Gate Array :
“An ASIC made to be configurable by user”

Hardware description Language
(Verilog, VHDL…)

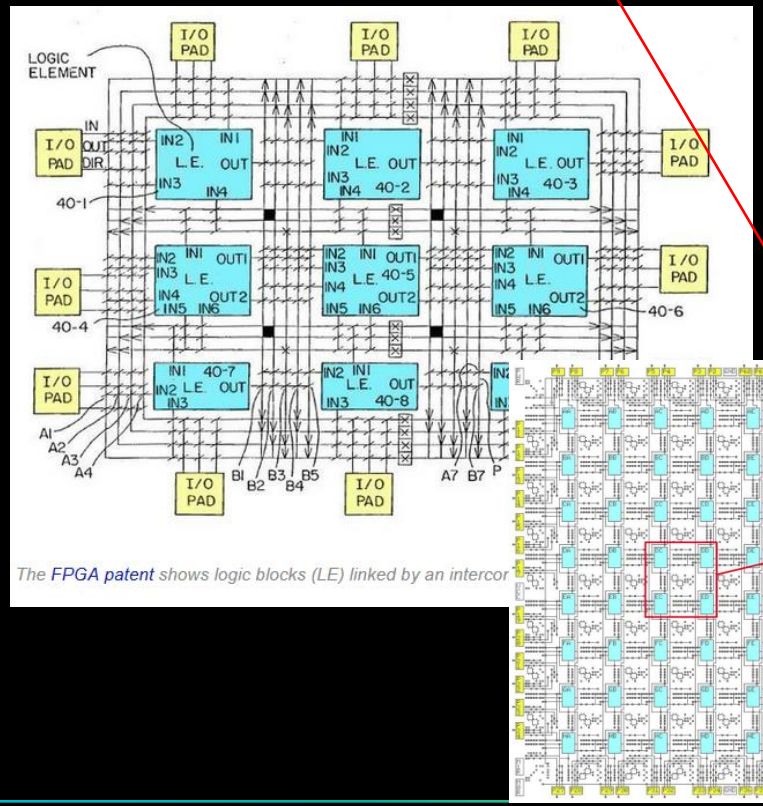
Synthesis / Place /route





Bitstream

```
Xilinx LCA BAR.lca 2064LPC68
File BAR.rbt
Sat May  5 12:16:34 2018
Sat May  5 12:16:34 2018
Source
Version
Produced by makebits version 5.1.0
11111111001000000000001011100001011111
01110101111111011111111011111111111111101111111101111111011111111111111111
01110110111111011111111011111111111111101111111101111111011111111111111111
01111111111110111111110111111101111111011111110111111101111111111111111111
01111111111111111111111111111111111111111111111111111111111111111111111111
01111111111111101111111101111111011111110111111101111111011111111111111111
01111111111111111111111111111111111111111111111111111111111111111111111111
01111111111111111111111111111111111111111111111111111111111111111111111111
01111111111111111111111111111111111111111111111111111111111111111111111111
```



https://github.com/f4pga/prjxray
https://www.righto.com/2020/09/reverse-engineering-first-fpga-chip.html

FPGA 2/2

Different flavors

Bitstream

```
Xilinx LCA BAR.lca 2064LPC68
File BAR.rbt
Sat May  5 12:16:34 2018
Sat May  5 12:16:34 2018
Source
Version
Produced by makebits version 5.1.0
11111111001000000000001011110000011011111
01110101111111011111111101111111111111110111111110111111101111111111111111
01101101111111011111111101111111111111110111111110111111101111111111111111
01111111111110111111110111111101111111011111110111111101111111011111111111
01111111111111111111111111111111111111111111111111111111111111111111111111
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01111111111111111111111111111111111111111111111111111111111111111111111111
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01111111111111111111111111111111111111111111111111111111111111111111111111
```
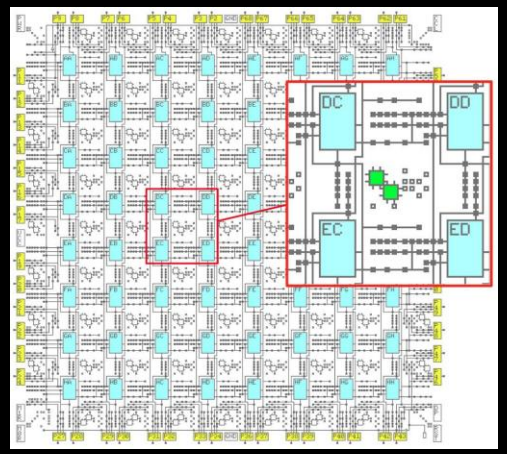



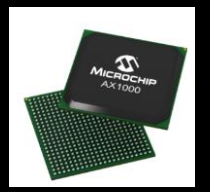
- **Antifuse based**
  - One time programmable
  - Live at power up
  - Totally robust to radiation
  - No companion memory
- **Flash based**
  - Live at power up
  - Low power consumption
  - “Configuration robust to radiation”
  - No companion memory

Non volatile configuration

- **SRAM based**
  - Need a companion non-volatile-memory
  - Fast
  - High density
  - High power consumption

Volatile configuration

Xilinx versal : 7nm

RadHard	RadTol
 130 nm	 150 nm
 65 nm	 28 nm
 65 nm	 20 nm

SOC / NOC

FPGA + PROCESSOR = SOC

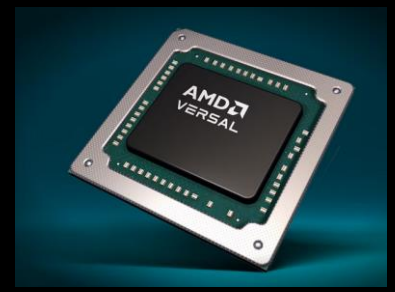
SOC + INTERCONNECT = NOC

SOC : System-On-Chip

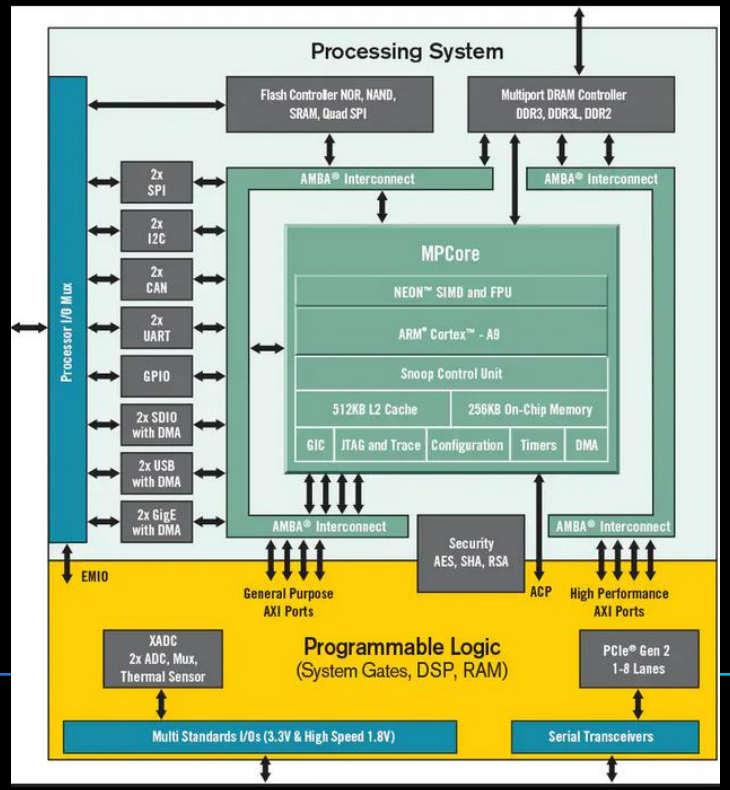
ex : Xilinx Zynq

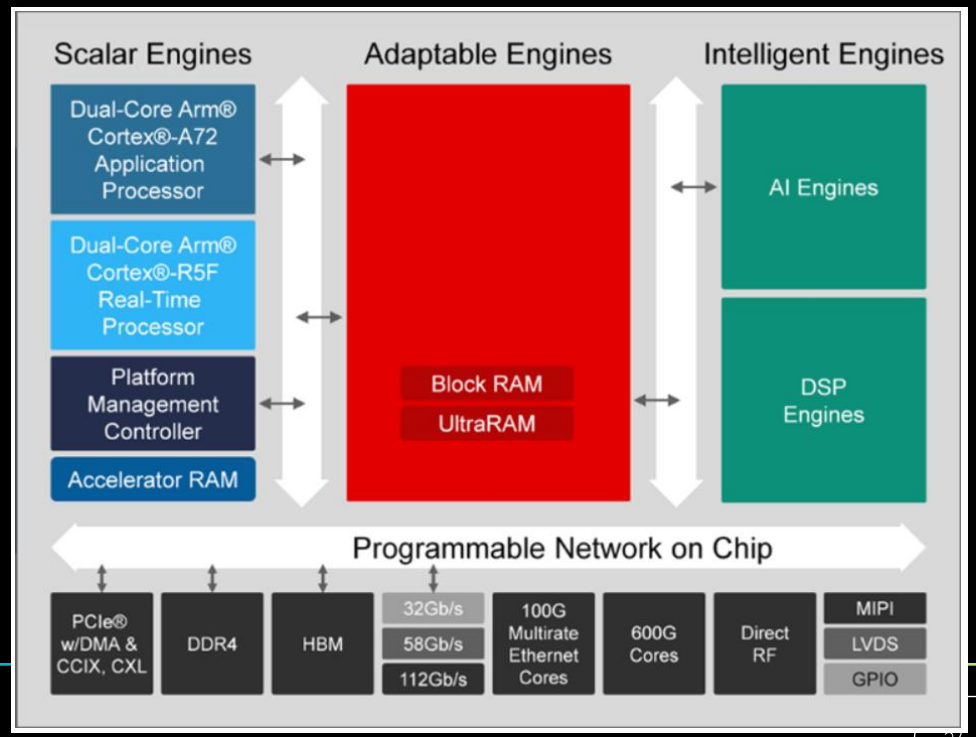
ex : Nanoxplore Ngultra

NOC : Network On Chip



ex : Xilinx Versal





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GANIL
Proton Therapy Center
Serbia
CERN
Croatia
TRAD
Rome
Tyrrhenian Sea

TIMELINE EXAMPLE BASED ON ZYNQ EVALUATION

START
Eyesat

Performance

generic software, Multicore, Radiologiciel, Generic Argos 4, AD9361, GNSS, Rover, Argos 4 optimized, Compression Eyesat

2013 2014 2015 2016 2017 2018

Tests

latchup, SEU #1, TID, Meca/ Thermal, SEU #2, laser, IR, Mixed field CHARM, laser injection, CEM

2013 2014 2015 2016 2017 2018

Architecture

Ninano: Nina, IoController, Serpentine

Ninano EM: GNSS Hypérion, Surveillance spectre, DMT/DT2, NanoTMHD-BX DVB-S2, GPS/Gallileo, Doris + GNSS

Ninano FM: Avionique intégrée, Hyperviseur, TM bande KA

2013 2014 2015 2016 2017 2018

Projects

ACDC, Leonidas, Argos Neo, CO3D, MMX, Angels, Darwin PF, Attipic

2013 2014 2015 2016 2017 2018

Eyesat

Timeline established in 2018 based on start on activities