20/11/2025

European Cyber Week
by CYBER
THE SOVEREIGN CYBER & DEFENCE AI FORUM

FOCH Project

Development of a fault-tolerant IP and evaluation of FPGA SRAM with tests in a highly radiative environment

ALP KILIC

NanoXplore

FLORENT MILLER

Nuclétudes

ALEJANDRO URENA-ACUNA

Radiation engineer at ONERA

JOSEPH PATUREL

INRIA

TABLE RONDE

FOCH Presentation

20/11/2025

9h20-9h50

REFECTOIRE

FOCH
global
Presentation

20/11/2025
9h20-9h50

Refectoire

Alp KILIC
NanoXplore

Development of a fault-tolerant IP and evaluation of FPGA SRAM with tests in a highly radiative environment

FOCH_A 100% French project

Project presentation

Coordinator

NanoXplore

NX Subcontractor

nucletudes arianeGROUP

2 french partners

Inria

ONERA THE FRENCH AEROSPACE LAB

Beginning of the project: 06/2024

End of the project: 09/2027 (36 months)

Funding: DGA

Project presentation

Manufacturing issues and process variations strongly affects the electrical parameter of circuits and architectures, leading to a significant reduction in manufacturing yields.

Transient errors caused by particles or radiation occur more frequently during operation, and process variability will prevent accurate prediction of chip performance.

Many systems are constantly under attack from intruders, and security has become of utmost importance.

Main objectives :

1. Evaluate NX FPGA SRAM technology linked to heavy radiative environments (such as aeronautical environments, launchers and defense environments).
2. Develop a RISC-V fault-tolerant IP.
3. Compare the analysis performed under particle beams or by laser injection. RISC-V processor validation and qualification.
4. Compare the sensitivity and performance of RISC-V processor IP carried on the NX FPGA target and on a state-of-the-art commercial FPGA target.

NanoXplore

European Leader in FPGA, Soc FPGA & ASIC Design

- French Based Company : Paris, Montpellier, Grenoble
- 140+ Employees with more than 90% R&D Engineers
- Offer products for Hi-Rel markets
- 3 different products offering :
  - High reliable SoC FPGA
  - ASIC design services
  - Silicon IPs
- ITAR Free Technology
- Focus on Space & Defense markets

NanoXplore

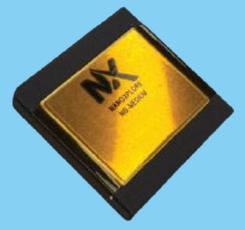
Products Overview

NG medium

Low-End FPGA

35kLUTs/32kDFFs
2.6Mb RAM
112 DSP
SpaceWire PHY
High Level SEU Rate

- Companion chip



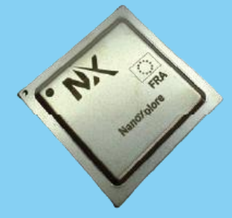
ESCC9000 qualified

ultra 300

Mid-End FPGA

290kLUTs/273kDFFs
21Mb RAM
896 DSP
16x HSSL 12G
ADC/DAC

- Payload
- Platform
- Sensor control
- Power control loop



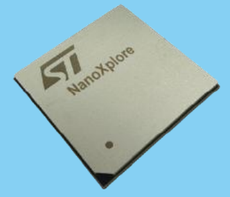
ESCC9030 expected

NG ultra

High-End FPGA

537kLUTs/505kDFFs
32Mb RAM
1344 DSP
32x HSSL 12G
Quad-core ARM-R52 (SoC)

- Payload
- Platform



ESCC9030 expected

65 nm

28 nm

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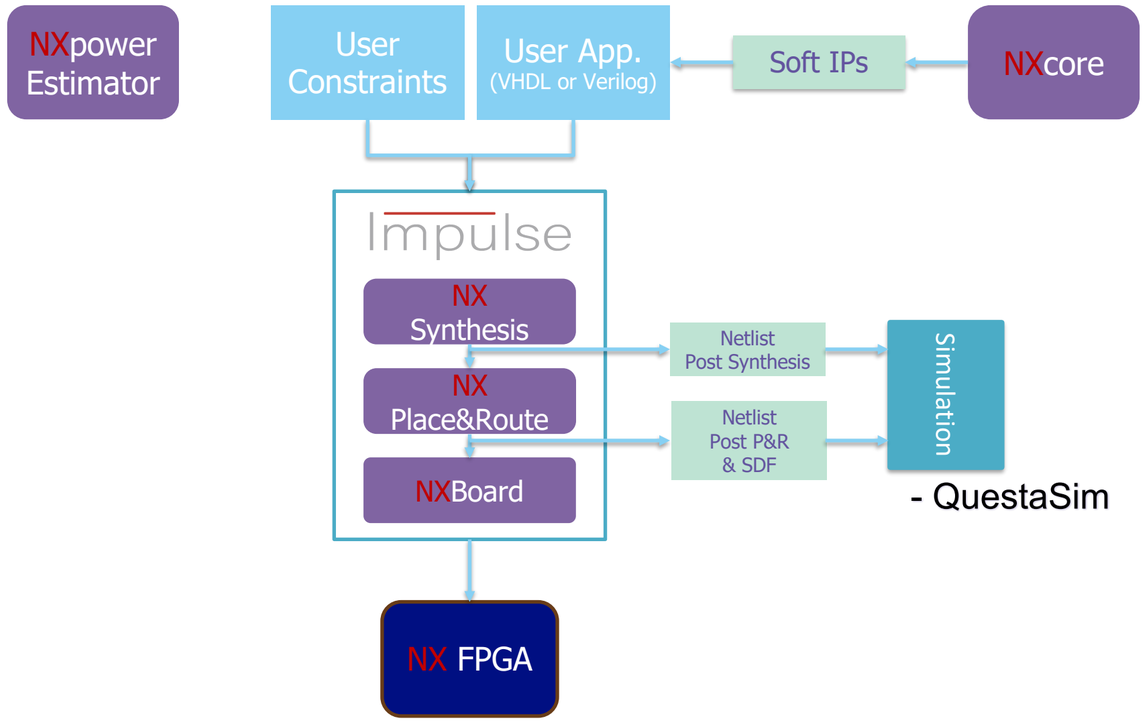
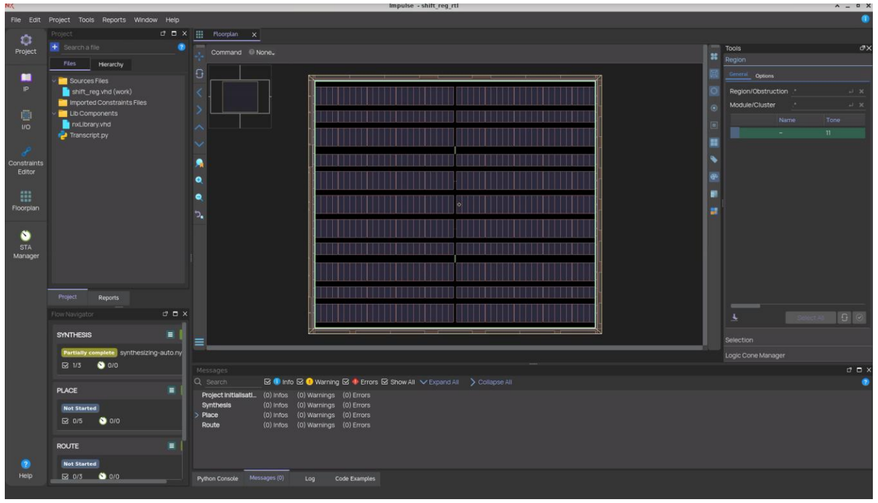
NanoXplore

Impulse FPGA Flow



: User input
: NX Software
: 3rd party Software
: Output file



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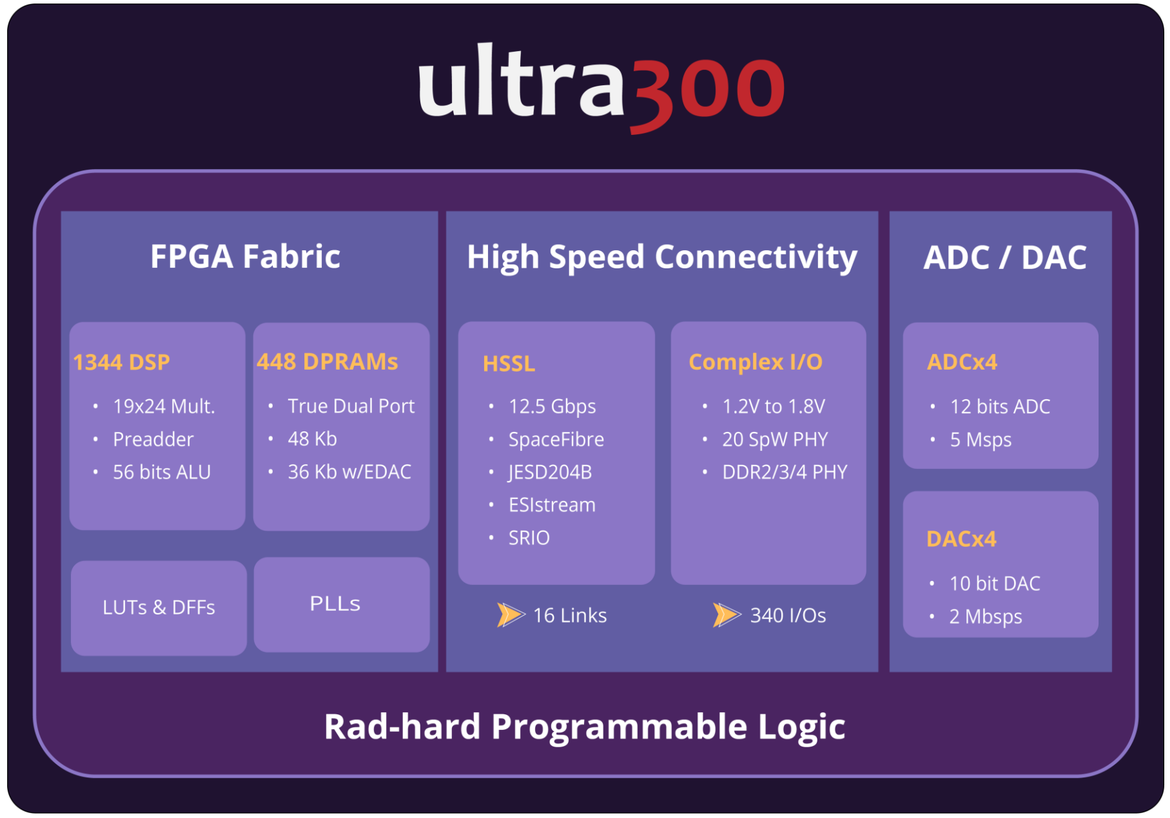
NanoXplore

ULTRA300 Rad Hard



- All-rounder
  - ✓ Small form factor with FCBGA-484
  - ✓ High pin count with FCBGA-1152
- Benefits from NG-ULTRA experience
  - ✓ FPGA Fabric
  - ✓ High Speed Connectivity
  - ✓ Radiation Performance*
  - ✓ Ecosystem
  - ✓ ... and more

* Configuration Memory: 0 errors up to LET 62 MeV*cm²/mg

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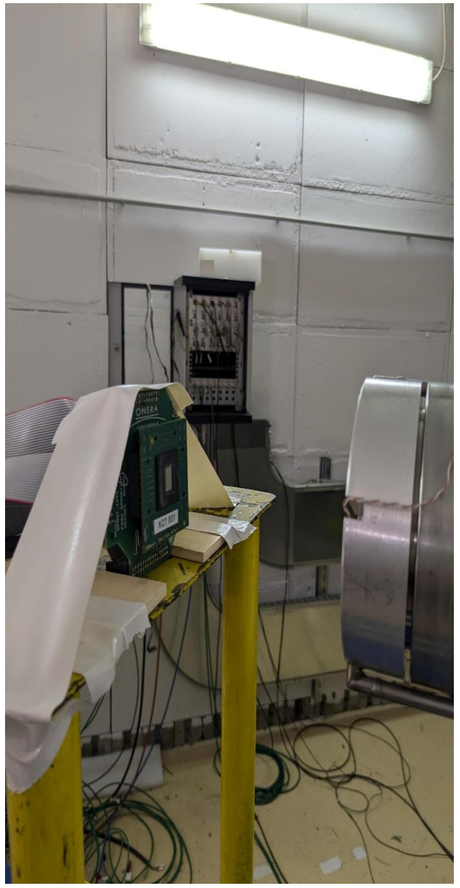
Refectoire

Alejandro URENA-ACUNA

ONERA

Development of a fault-tolerant IP and evaluation of FPGA SRAM with tests in a highly radiative environment

ONERA ECM team



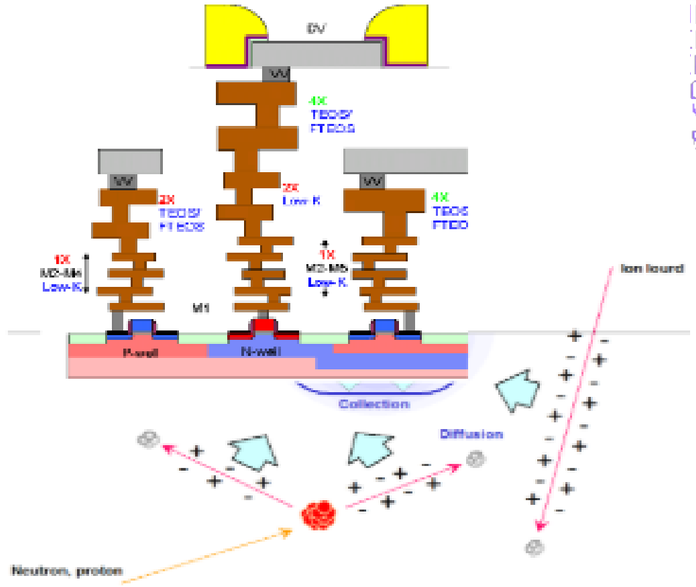
Experimental evaluation of COTS and ASICs

ECM team composed of:

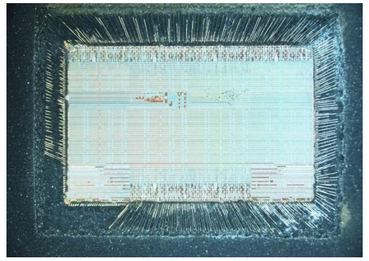
- 13 Permanents
- 10 Phd students
- 1 post-doc

Main activities:

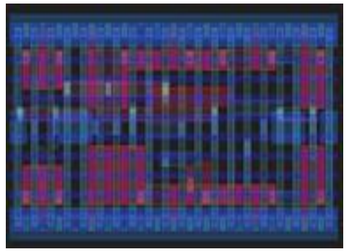
- Radiation effects in materials and microelectronics devices
- Strong experience in diagnosing radiation response of COTS and ASICs through experimental and simulation means by using the fault injection technique (MUSCA SEP3 + TERRIFIC)
- SEE characterization in deep technological nodes (ex. 65 nm bulk , 7nm FinFET, 28nm FDSOI)



Particle-Semiconductor interaction



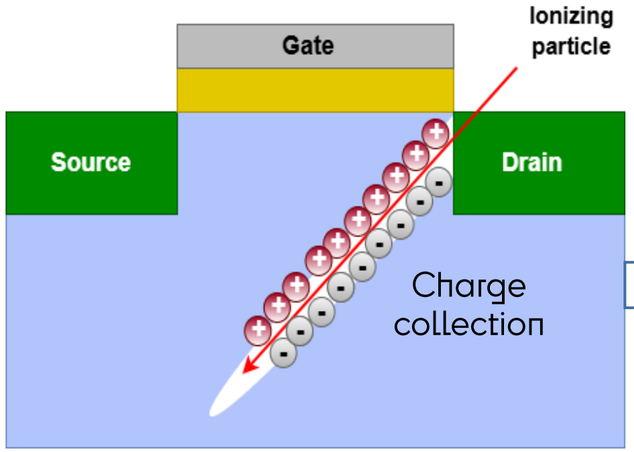
Top view of an ASIC



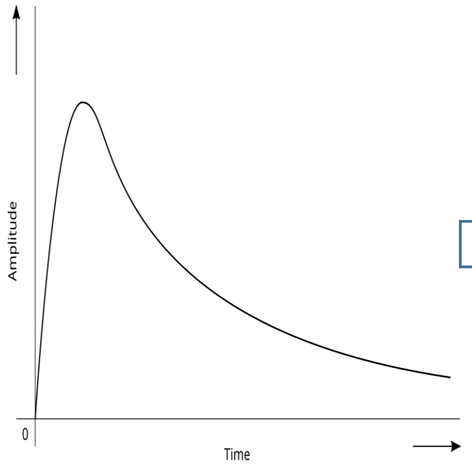
Circuit layout

Introduction: Radiation effects in electronics

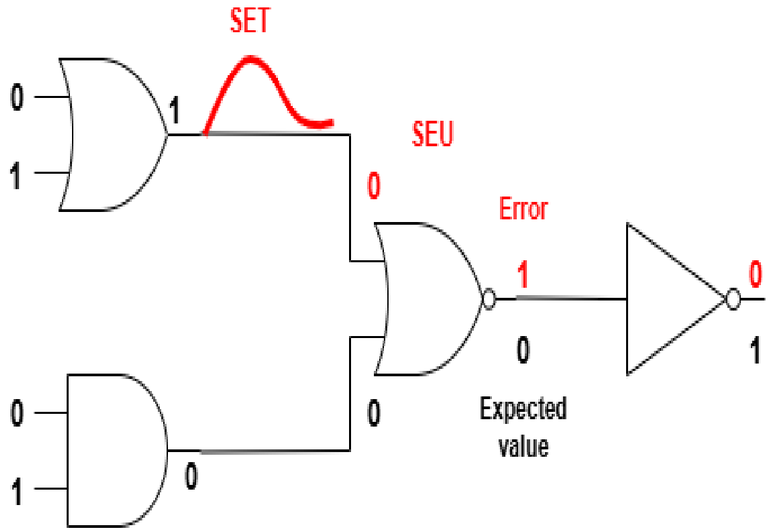
MOS transistor



Bulk, SOI, FinFET



Single event transients (SET's)



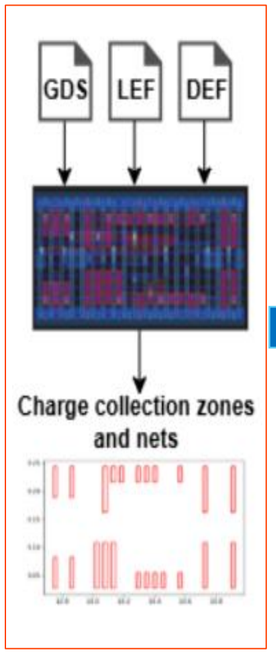
Errors in combinational and sequential logic

Scope of ONERA

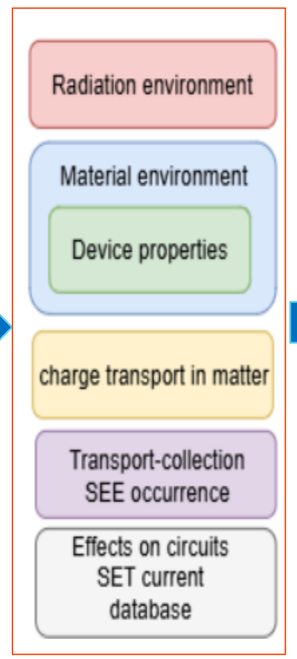
SEE
- Single event transients (SET)
- Single event upset (SEU)
- Multiple event upset (MBU)
- Multiple cell upsets (MCU)

ONERA Simulation flow: MUSCA SEP3 + TERRIFIC

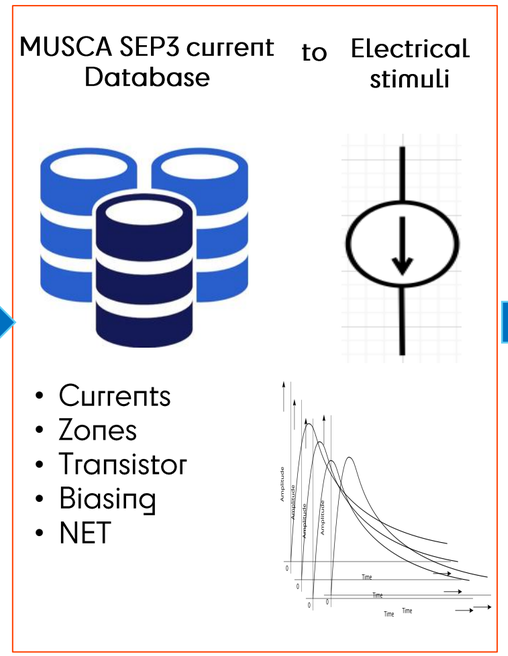
Circuit analysis



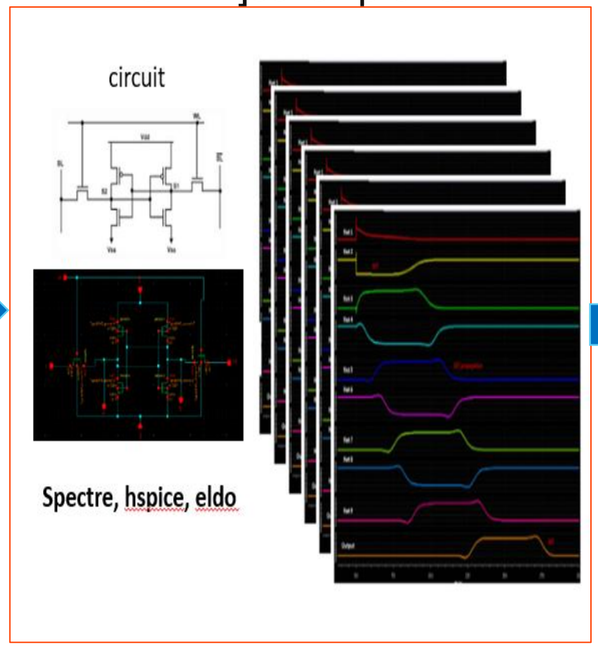
MUSCA SEP3



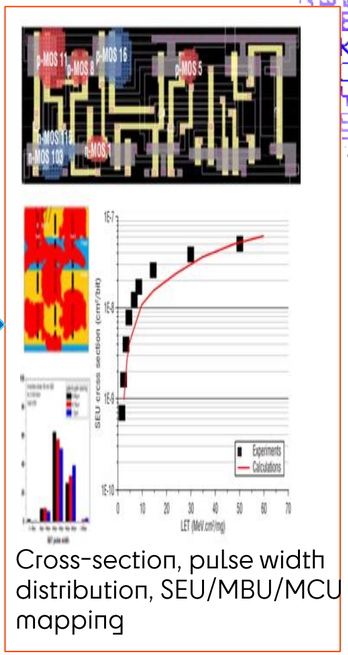
Stimuli generation



TERRIFIC : Fault injection platform



Post-processing

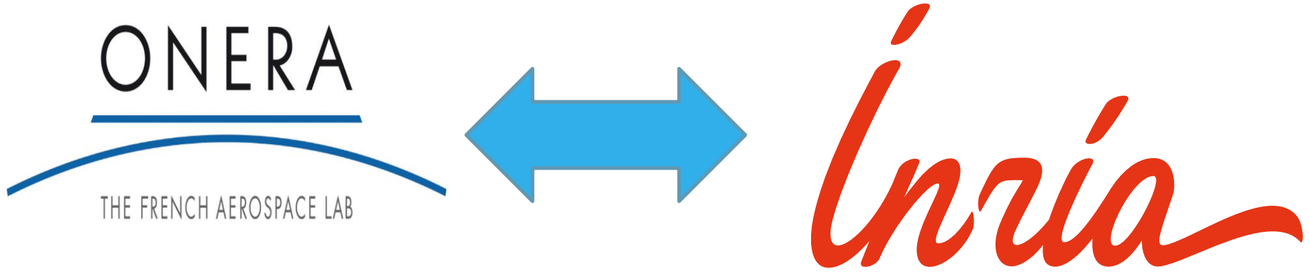


Cross-section, pulse width distribution, SEU/MBU/MCU mapping

The MUSCA SEP3 coupled with TERRIFIC simulation flow is also effective in determining MBUs and MCUs in deep technological nodes: ex. 7nm FinFET

ONERA's goals in FOCH Project

- Evaluation of Nanoxplore digital cells with the MUSCA SEP3 and TERRIFIC simulation tools.
- Generation of an SET current database through MUSCA SEP3
- Simulation of the radiation response digital blocks such as the configuration memory, DFFs, and LUTs
- Definition of a fault injection formalism with INRIA for an RTL-level fault test



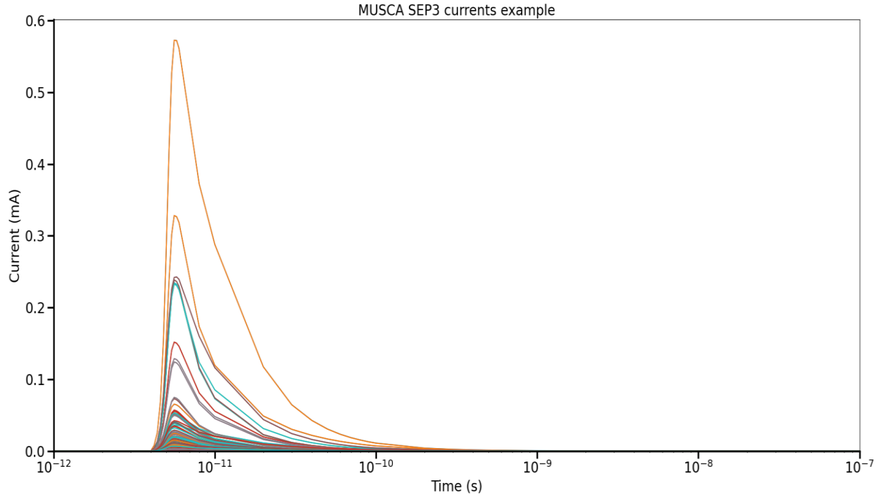
First results of ONERA SEE evaluation for EOCH

Evaluation of Nanoxplore digital blocks:

- Configuration memory
- DFFs
- LUTs

Results and first conclusions

- No errors observed under a 23 MeV neutrons SET database
- Confirms the Nanoxplore FPGA robustness
- New databases will be generated including protons and heavy ions in order to test the FPGA robustness
- Need of experimental data to confirm the obtained results



Examples of MUSCA SEP3 generated SETs

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9h20-9h50

Refectoire

FLORENT MILLER

Nuclétudes

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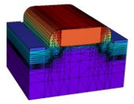
NUCLETUDES IN THIS CONSORTIUM



Task-1

Multi-layer analysis by simulation of the fault tolerance of the NX target FPGA

NanoXplore
ONERA THE FRENCH AEROSPACE LAB
Inria

Task-2

Experimental characterization of the fault tolerance of a RISC-V IP implemented on two different FPGA targets

nucletudes arianeGROUP

- Design elementary tests
- Prepare fault injection
- Perform experiment
- Analyze results

Task-3

Implementation of hardening strategies on the RISC-V IP

nucletudes arianeGROUP

- Knowledge in hardening strat.
- Knowledge in RISC-V IP archi.
- Complementary tests (ex: laser)
- Analyze fault injection

Task-4

Experimental validation of the benefit of the implemented hardening strategies on the RISC-V IP

nucletudes arianeGROUP

- Design elementary tests
- Prepare fault injection
- Perform experiment
- Analyze results

As expert in radiation experiments with a strong knowledge on testing complex components

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NUCLETUDES IN THIS CONSORTIUM

Task-1

simulation … tolerance

NanoXplore

ONERA
THE FRENCH AEROSPACE

Inria

Task-2

Experimental characterization of the fault tolerance of a RISC-V IP implemented on two different FPGA targets

nucletudes
arianeGROUP

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arianeGROUP

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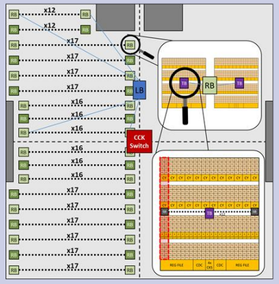
NUCLETUDES AS COORDINATOR OF FAULT INJECTIONS EXP.

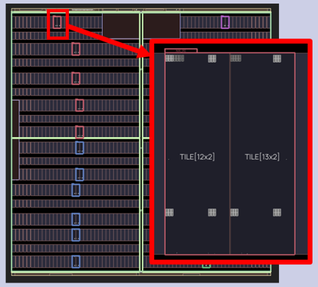
Tasks list overview:

T1 : [illegible] | T2 : Fault injections | T3 : Hardening Strategies | T4 : Fault injections

- Designing elementary tests on the targeted FPGAs

→ Ex: Rare but critical events requiring high flux



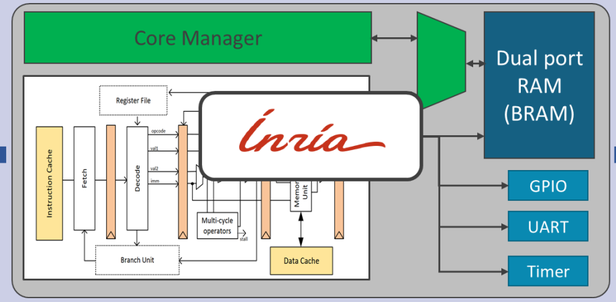


- Porting a RISC-V IP (Comet-V) for fault injections

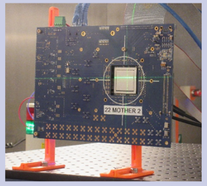
→ Comparing 2 FPGA : NX & state of the art flash based FPGA

FPGA ref n°1

Hybrid test board (modified)
→ ULTRA300 from NX



FPGA ref n°2



Nucletudes neutron test board
→ Other FPGA (not NX)

NanoXplore

User feedback on Impulse toolchain

Support for adding RISC-V IP in NX libs

Complete & compare radiation data

ONERA
THE FRENCH AEROSPACE LAB

Experimental data feedback for MUSCA SEP3 and TERRIFIC simulation tools on the UCL-NIF Facility

Inria

Functionality requests and user feedback for a wider adoption of the Comet-V core

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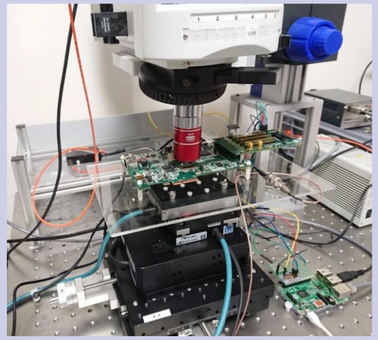
NUCLETUDES AS SUPPORT FOR HARDENING STRATEGIES

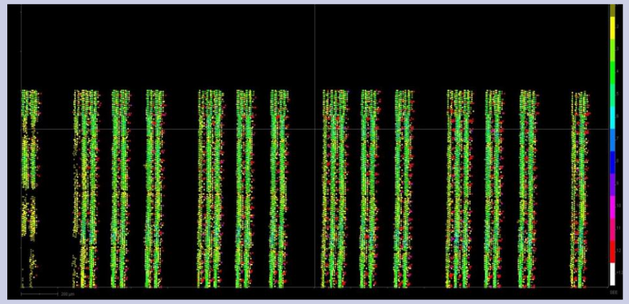
Tasks list overview:

T1 : [illegible] → T2 : Fault injections → T3 : Hardening Strategies → T4 : Fault injections

- **Dedicated fault injection test methods**

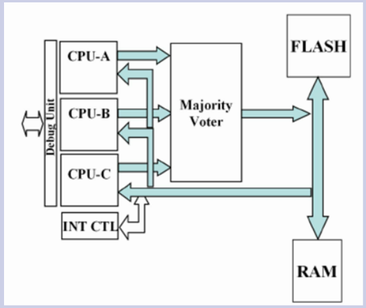
→ SPA Laser to accurately identify critical events & test mitigations

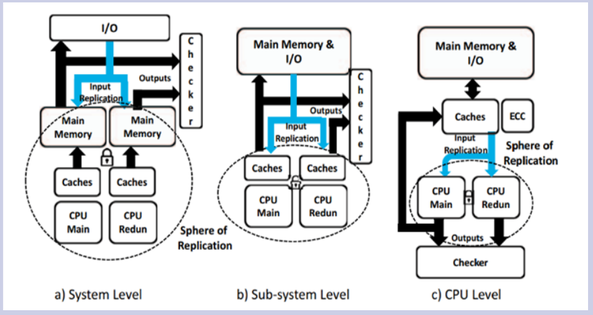




- **Support for RISC-V hardening techniques**

→ TMR, Cores Lock stepping, ECC, CRAM scrubbing, …





NanoXplore

User feedback on Impulse toolchain

Support for adding a fault tolerant RISC-V IP in NX libs

Support for identifying key resources requiring hardening

Inria

Support to identify vulnerable parts of the Comet-V core

Support to select the most suitable hardening methods

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Refectoire

JOSEPH PATUREL Inria

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Partner Presentation

Inria

TARAN team, Domain-Specific Computers in the post Moore's law era

- About 40 members, researchers, engineers and PhD students
- Automatically create hardware that is resilient, computes just right and leverages emerging technologies

Research direction: Resilient accelerators, CPUs and GPUs

- Vulnerability analysis at Design-time and Run-time, task-level scheduling strategies, exploring low-overhead techniques to protect architectures against faults (and attacks).

Building around the RISC-V ecosystem and open-source hardware

- Member of the RISC-V foundation
- Maintainer of the Comet core

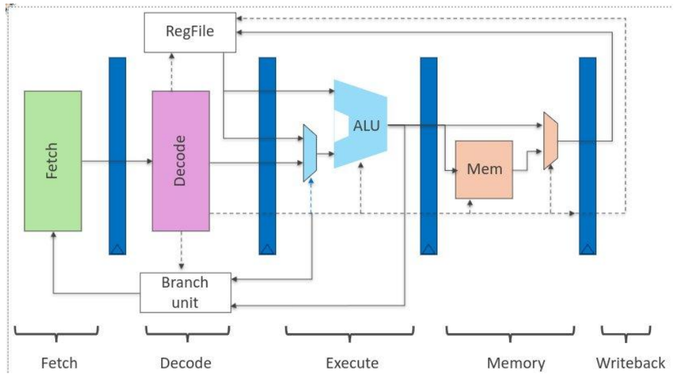
- Cross-layer vulnerability analysis of NanoXplore FPGA fabric
- Provide a fault-tolerant RISC-V processor IP

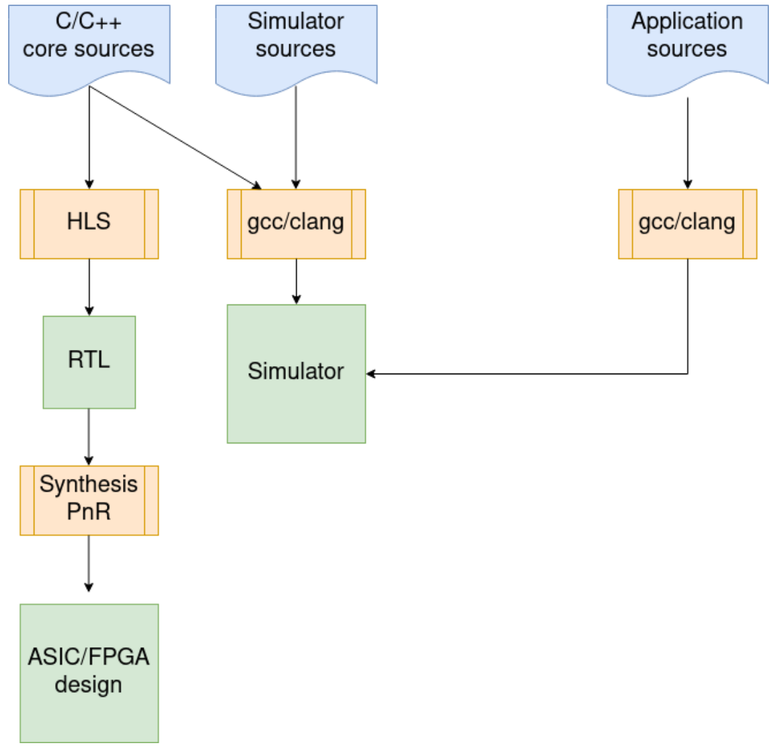
RISC-V Evaluation Platform

Comet[1]

Embedded class in-order, 5-stage pipelined RISCV 32-bit core written in C++

- M-extension, caches and standard IRQ support
- Easily modified using open-source and industry-standard tools





Used as a test platform for micraorchitectural research:

- Dependability[2], Security[3], Normally-Off Computing[4]

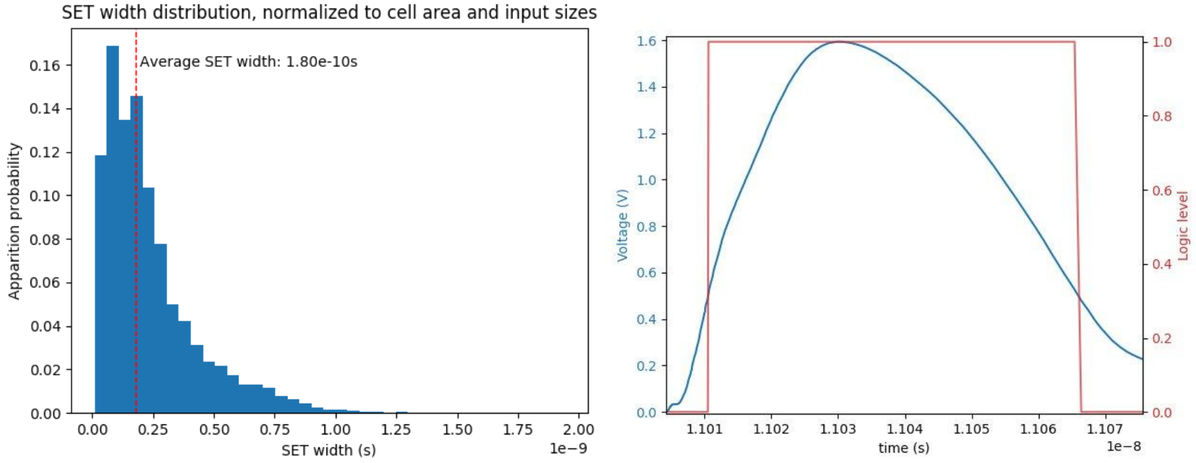
Developped an FPGA SoC around the core for beam-testing in tandem with Nuclétudes

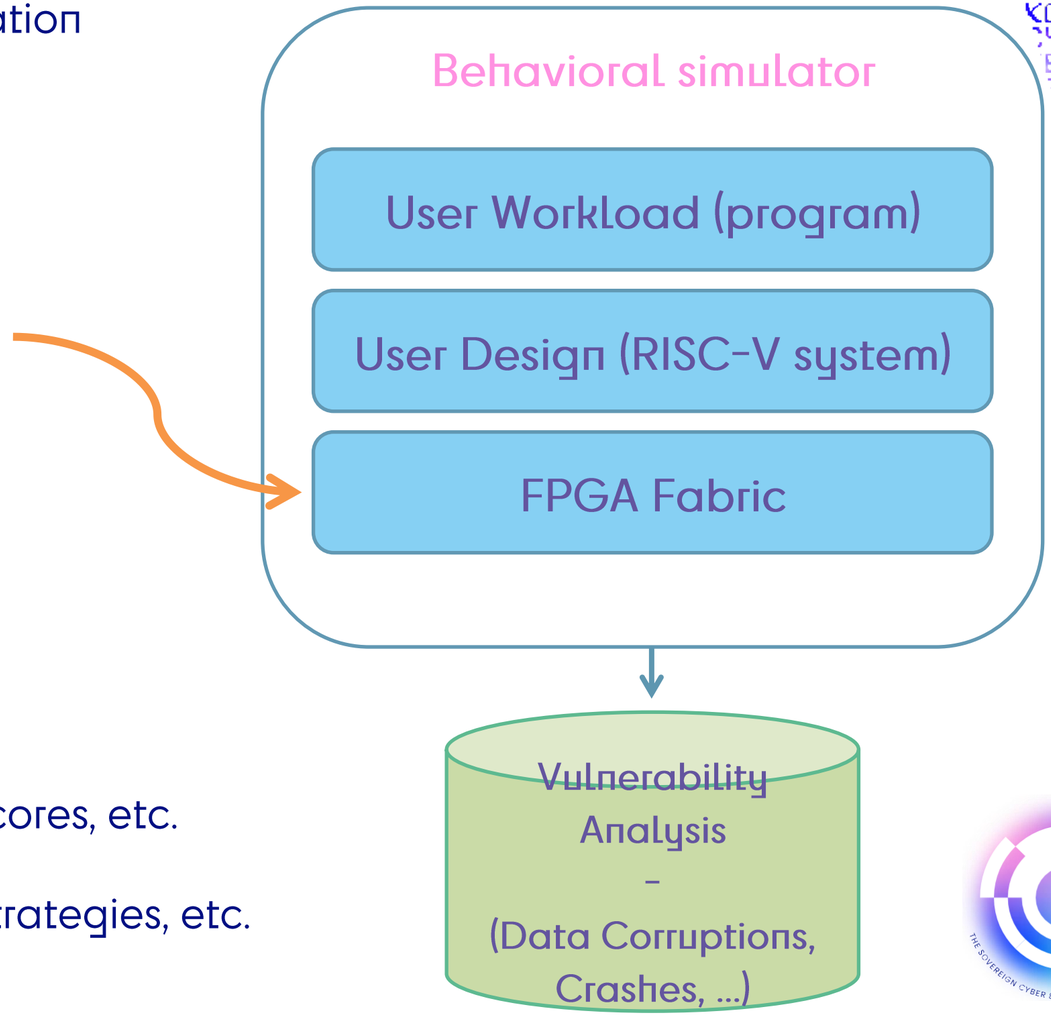
[1]: S. Rokicki, D. Pala, J. Paturel and O. Sentieys, "What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications", IEEE/ACM ICCAD 2019
[2]: P. R. Nikiema et al., "Towards Dependable RISC-V Cores for Edge Computing Devices," IEEE IOLTS 2023
[3]: L. Savary, S. Rokicki and S. Derrien, "Ahead of Time Generation for GPSA Protection in RISC-V Embedded Cores", IEEE ASAP 2025
[4]: D. Pala, I. Miro-Panades and O. Sentieys, "Freezer: A Specialized NVM Backup Controller for Intermittently Powered Systems," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2021

Vulnerability Analysis

Gate-Level Fault Injection

Inject fault profiles provided by Onera in a full-fabric simulation



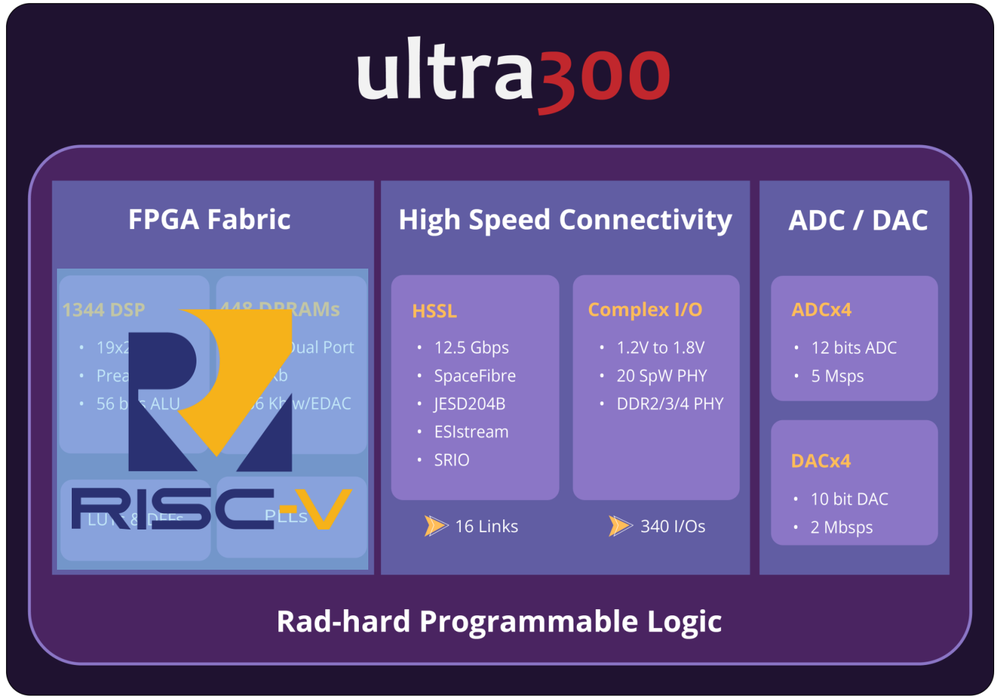


Allows us to efficiently guide selective hardening of:

- Software that is running on the core
- The CPU microarchitecture: ECC register file, lockstep cores, etc.
- The FPGA fabric: redundant routing paths, scrubbing strategies, etc.

Conclusion

- First test campaign: 23/12/2025



- Fault Tolerant RISC-V IP is planned to be available at the end of the project

Thank you