PhaseSCA

Exploiting Phase-Modulated Emanations in Side Channels

SemSecuElec October 24, 2025

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  EURECOM – Biot
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  EURECOM – Biot
- *Clémentine Maurice*
  Univ. Lille, CNRS, Inria – Lille

Introduction

Unintentional Emanations

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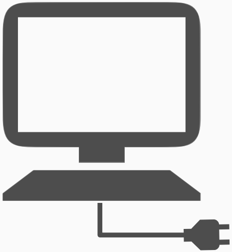
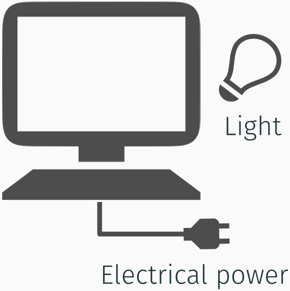


Electrical power

Unintentional Emanations



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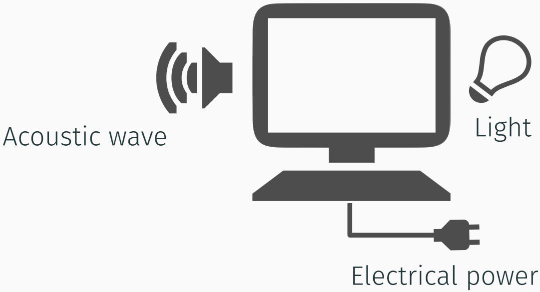

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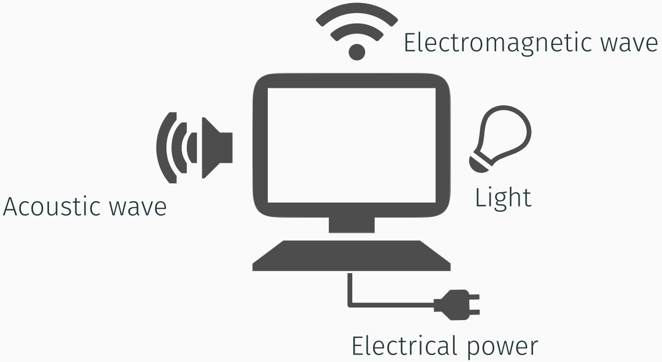

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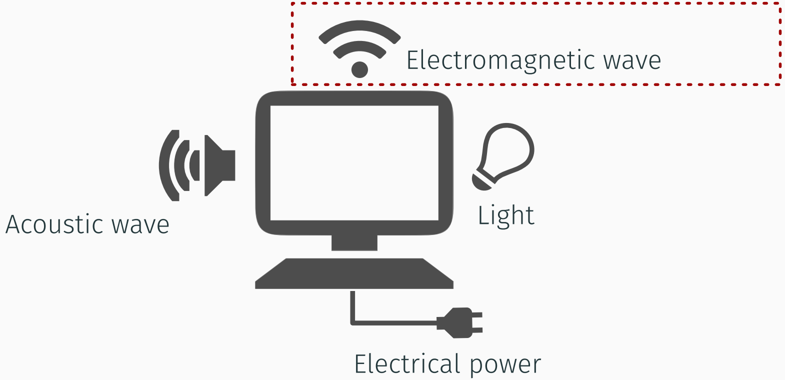
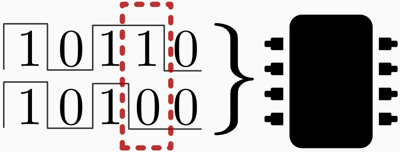


Compromising Emanations

Difference in the logic input



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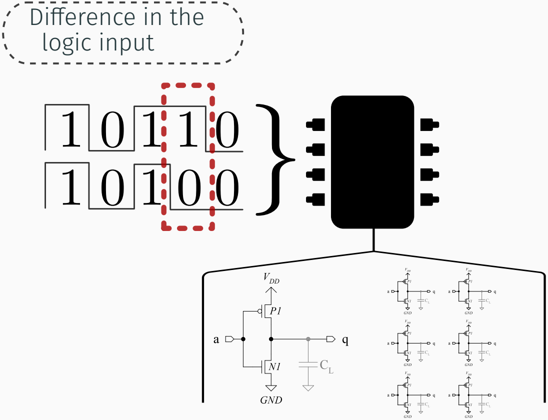

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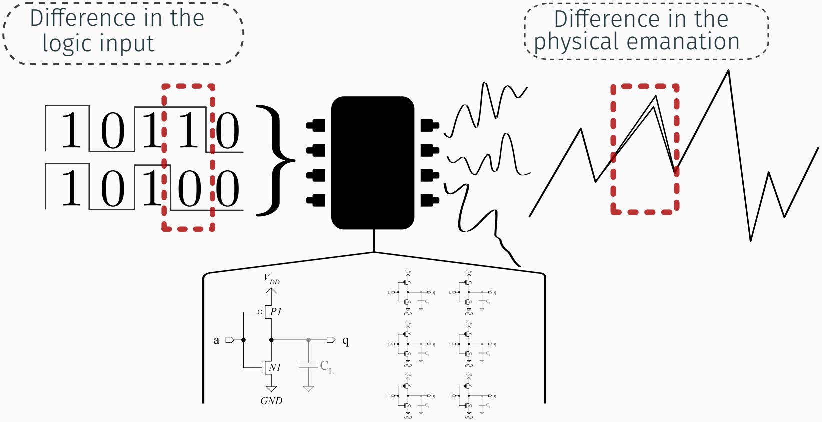
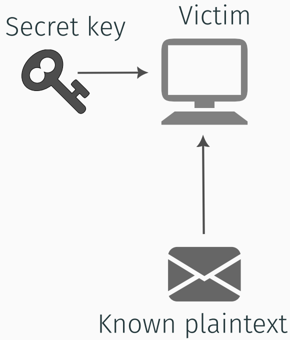


Example of a Side-Channel Attack



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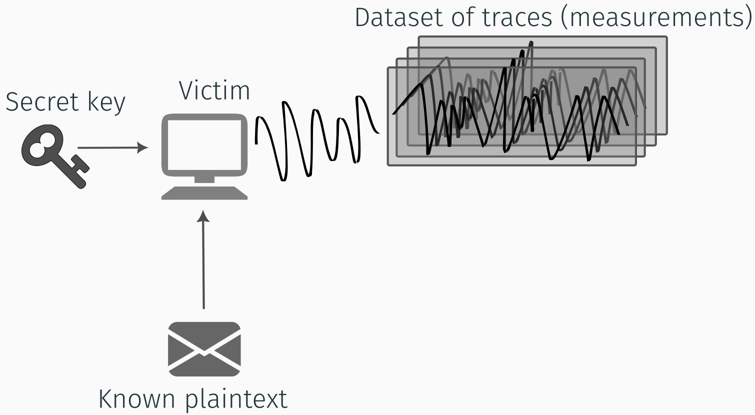

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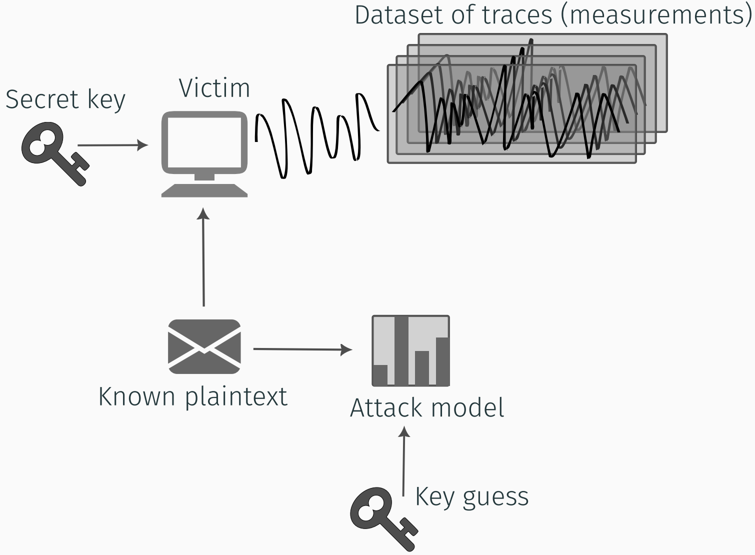

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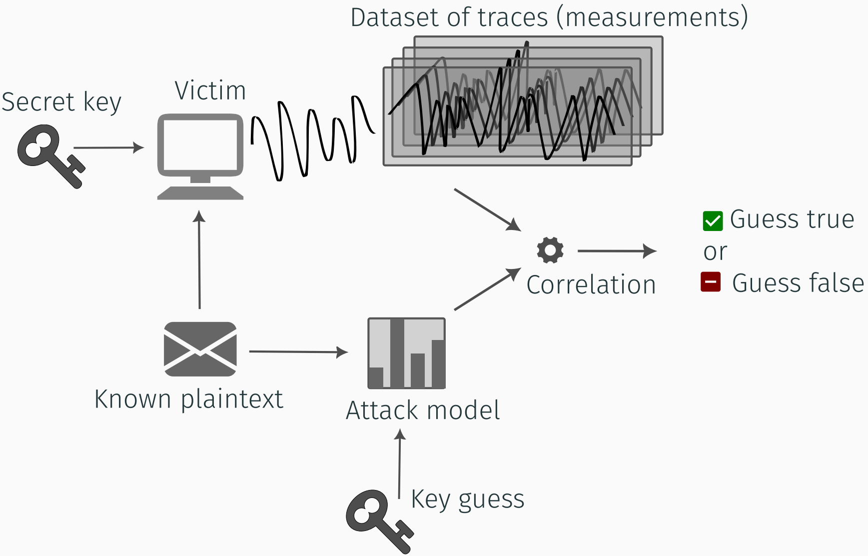
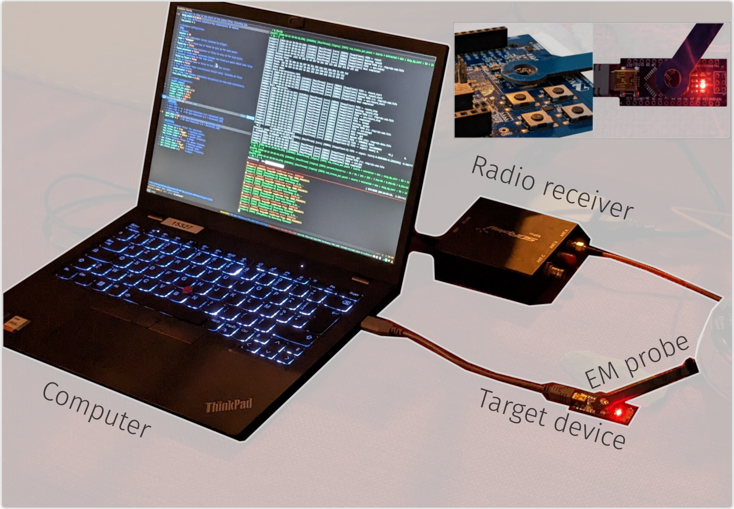


EM side-channel attack



Attacking an ATmega328 on a Arduino Nano and an nRF51422

Overview

Contribution

Demonstrating a novel side-channel leakage source through unintended phase modulation of electromagnetic signal

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Demonstrating a novel side-channel leakage source through unintended phase modulation of electromagnetic signal

Outline

1. Exploitation of phase in side channels
2. Analysis of the root cause phenomenon

Exploitation of Phase-modulated Side Channels

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Amplitude-modulated Emanations to Side-channel Trace

Proxy Traces – From Amplitude to Power

[QS01; VP09; Cam+18; WWD20; Gen+22]

EM Amplitude

Power

= Proxy

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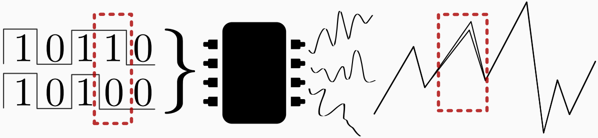

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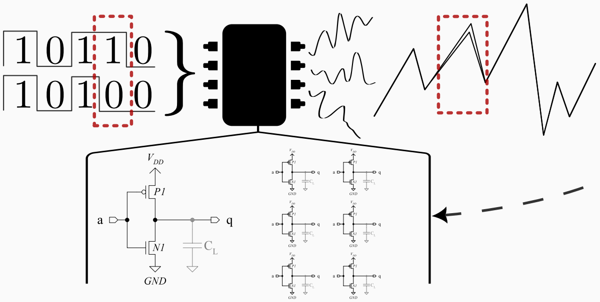

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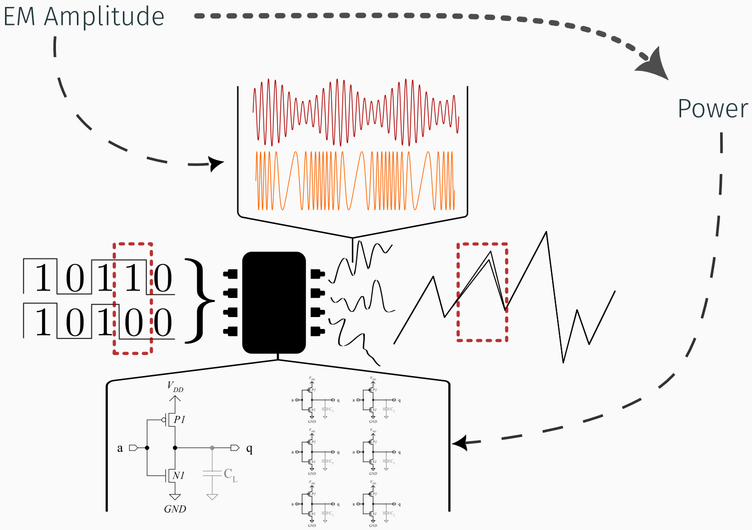
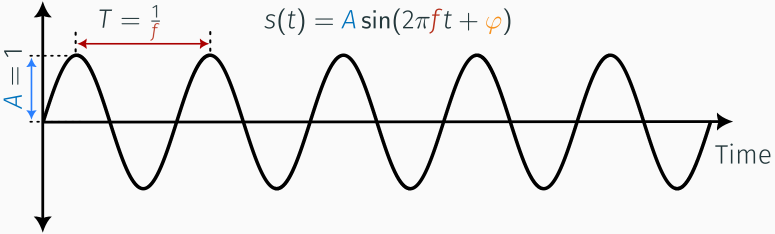


Amplitude in Signal Representation

Real-valued signal

$$s(t) = A\sin(2\pi f t + \varphi)$$



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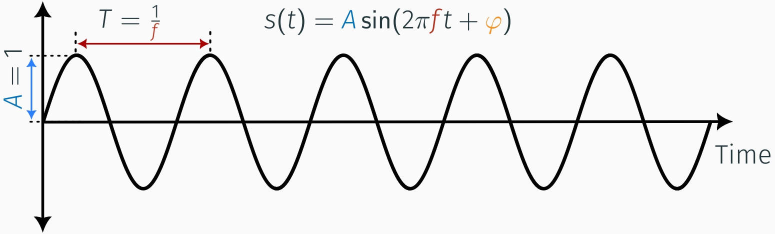

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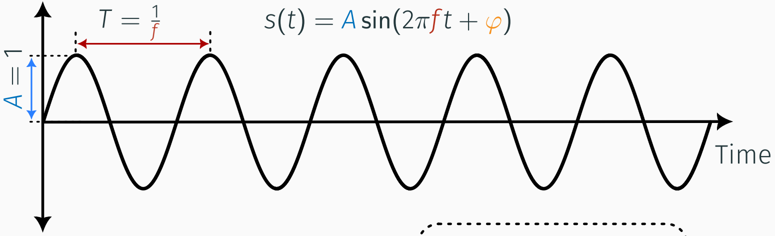

Complex-valued signal
(analytic representation)

$$\begin{aligned} s(t) &= I\cos(2\pi f t) + Q\sin(2\pi f t) \\ x_i &= I + jQ \end{aligned}$$

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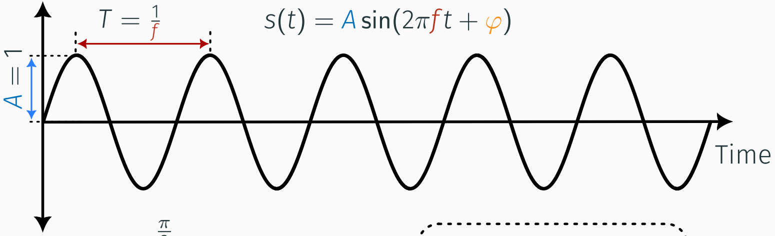

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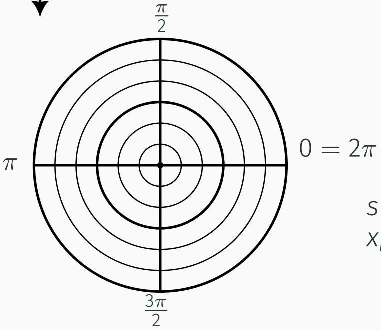

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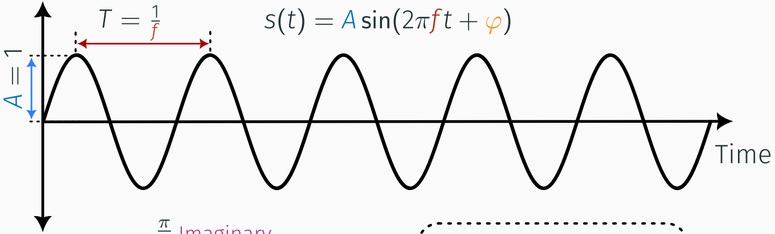

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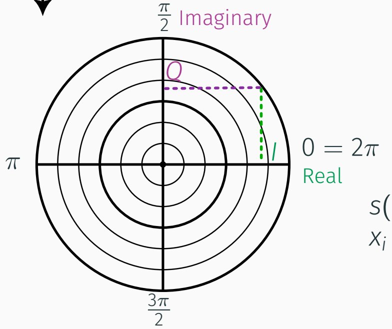

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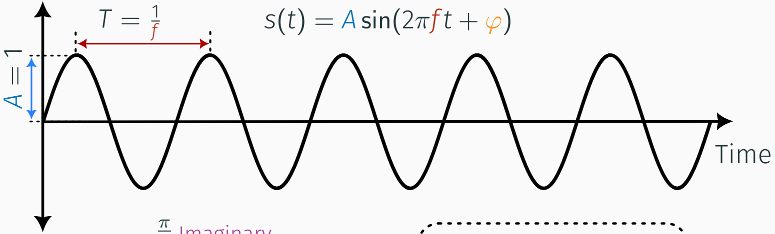

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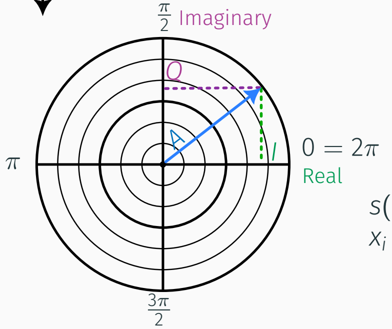

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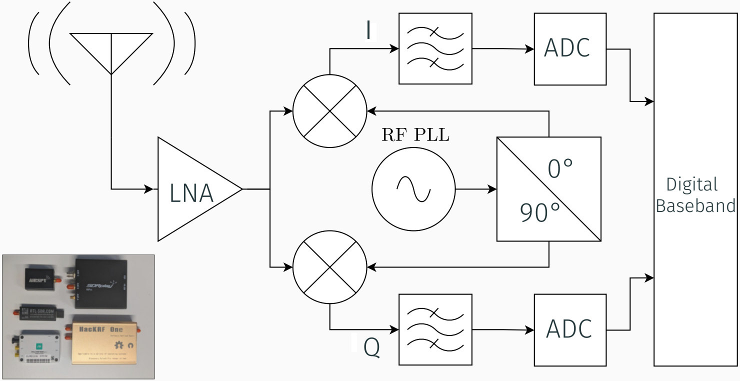
Simple SDR receiver Architecture

Various Software-Defined Radios (from 20$ to 1000$)

Simple SDR receiver Architecture



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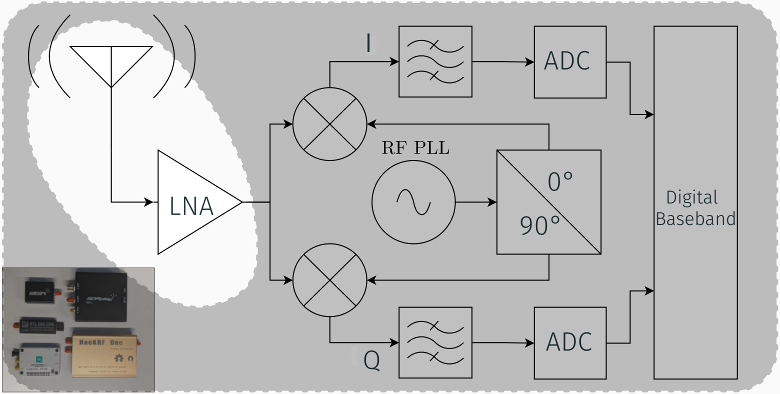

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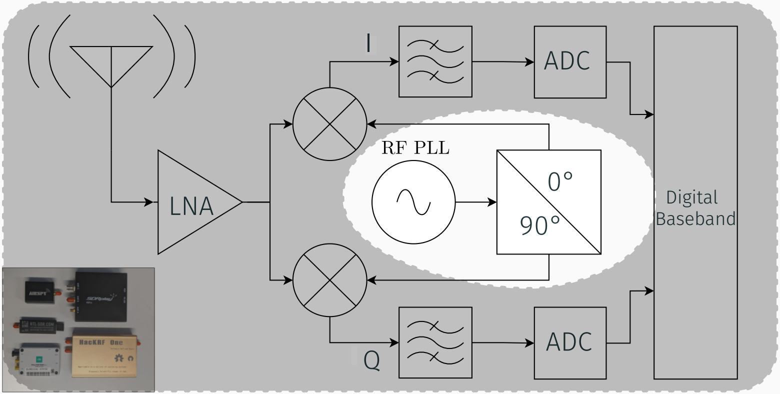

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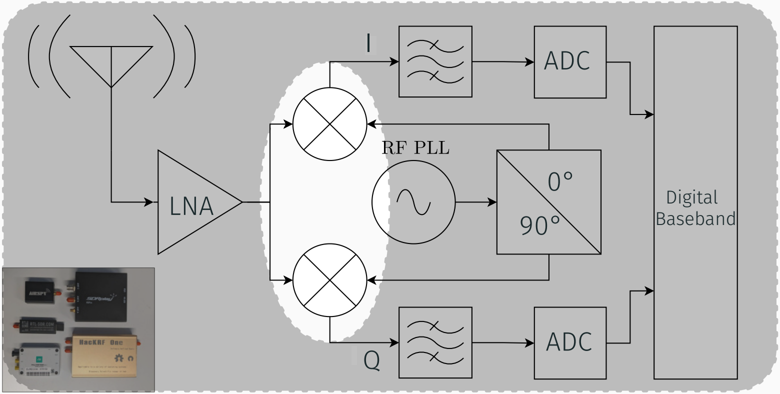

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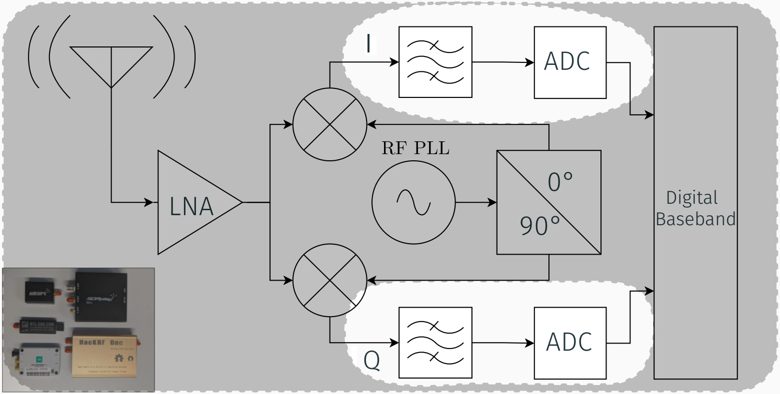
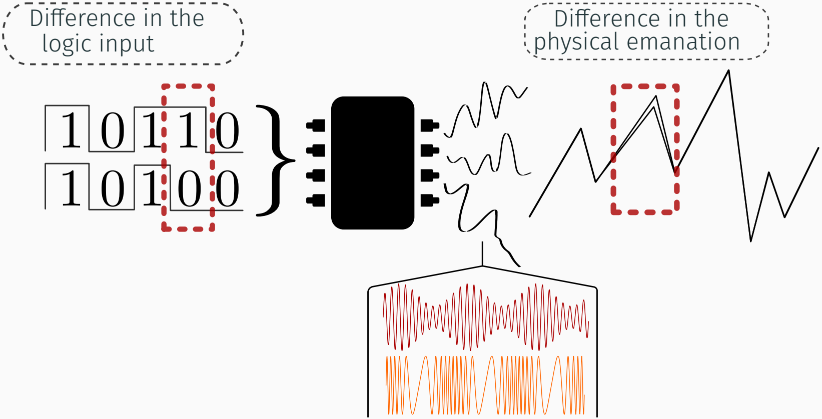
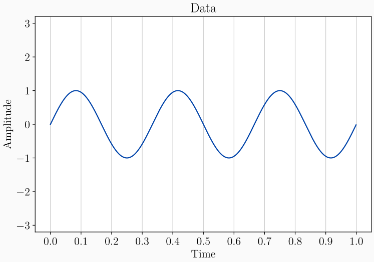


Modulations in Compromising Emanations



Amplitude Modulation (AM)



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$m(t) = A_m \sin(2\pi f_m t + \varphi_m)$

In EM side channels, **message** is related to the **secret**, **carrier** can be a **digital clock** for example

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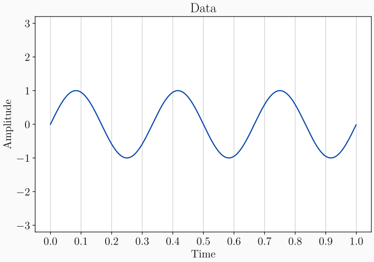

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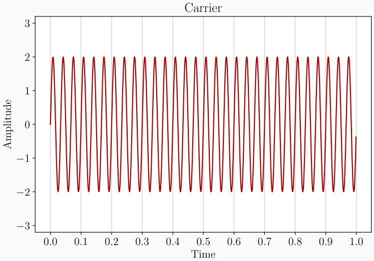

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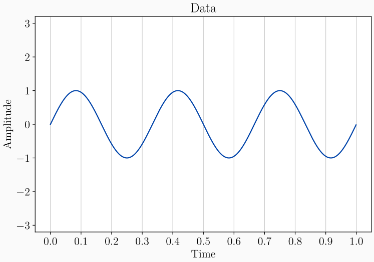

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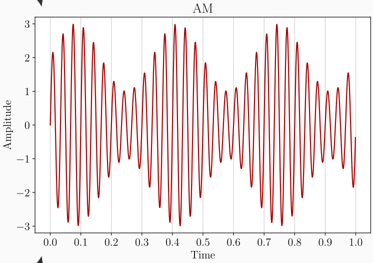
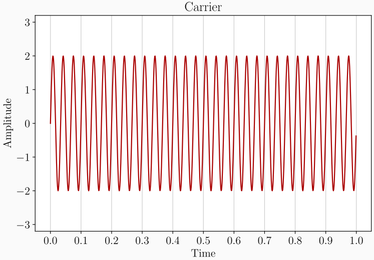


Amplitude-modulated carrier (Bandpass):
$y(t) = [A_c + m(t)]\sin(2\pi f_c t + \varphi_c)$



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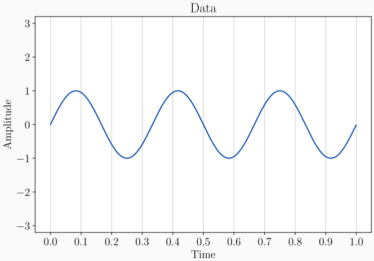

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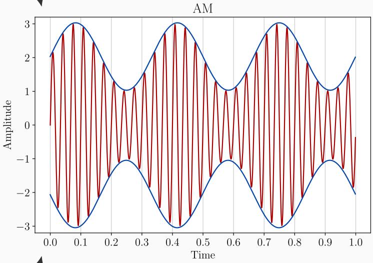

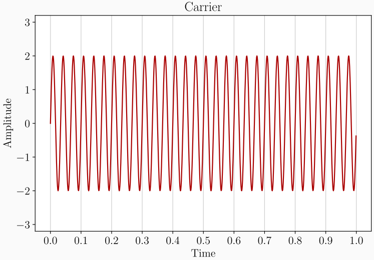

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Summarizing signal processing background

We know...

- How to represent a signal (using **IQs** *a.k.a.* analytic representation)
- How to measure a signal (using **SDRs**)
- How information is embedded inside a signal (through **modulation**)

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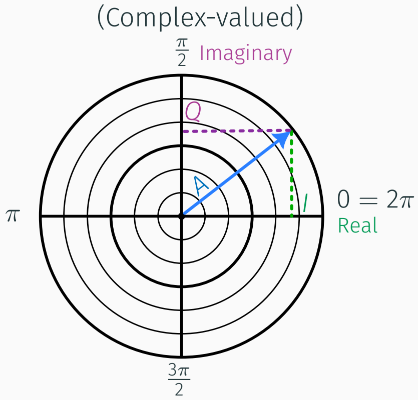
We can now...

1. Acquire our signals
2. Demodulate them
3. Perform a side-channel attack

Amplitude Trace Computation



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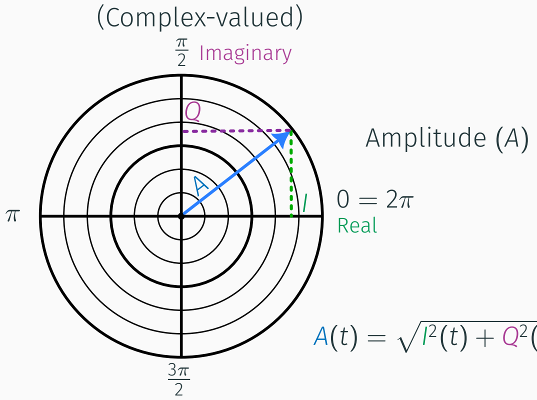

$$A(t) = \sqrt{I^2(t) + Q^2(t)}$$

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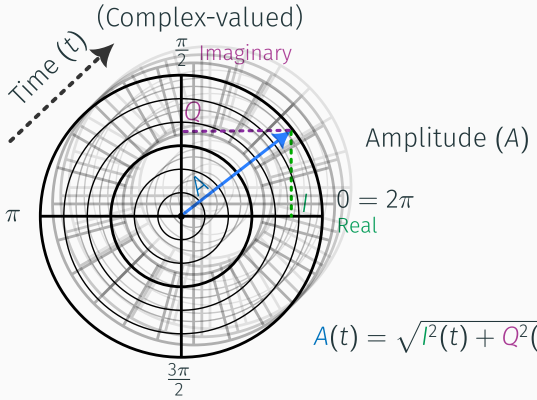

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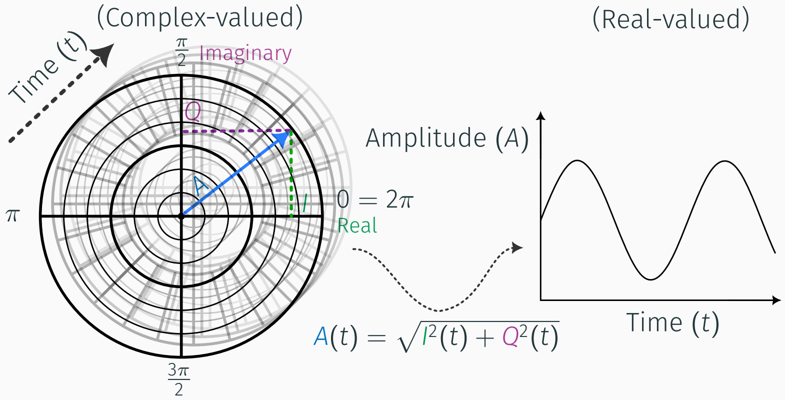
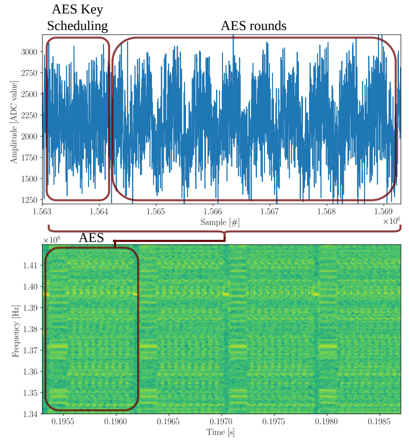


Visualizing AES in Amplitude Trace



Exploitation of Phase-modulated Side Channels

Phase-modulated Emanations to Side-channel Trace

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[QS01; VP09; Cam+18; WWD20; Gen+22]

EM Amplitude

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= Proxy

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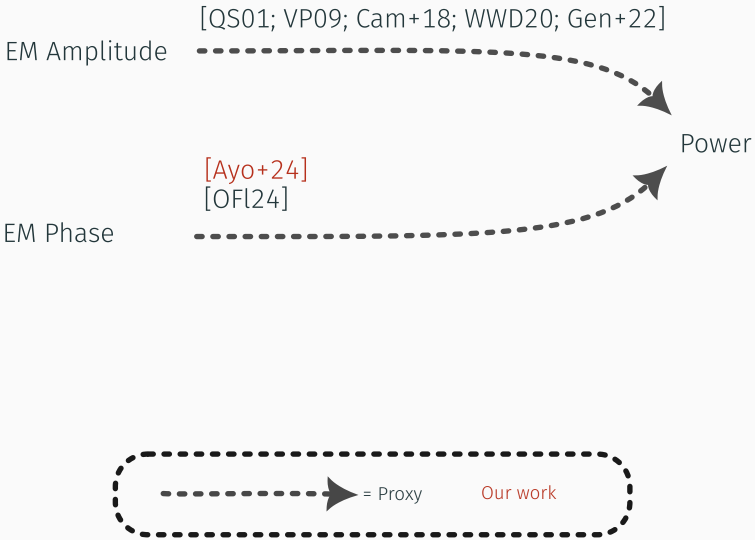

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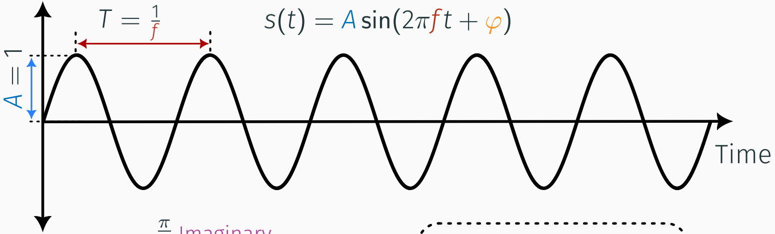
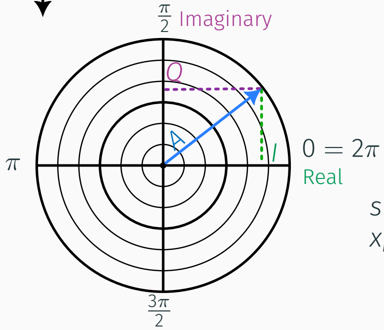


Complex-valued signal

(analytic representation)



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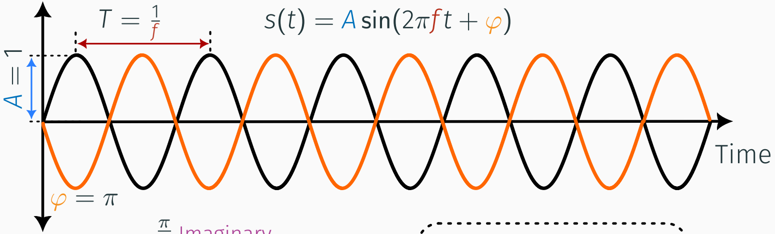

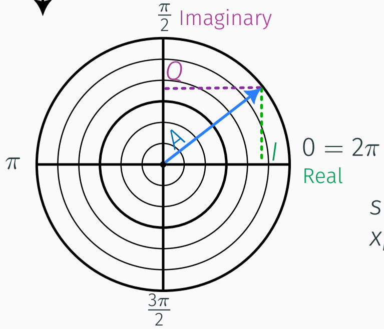

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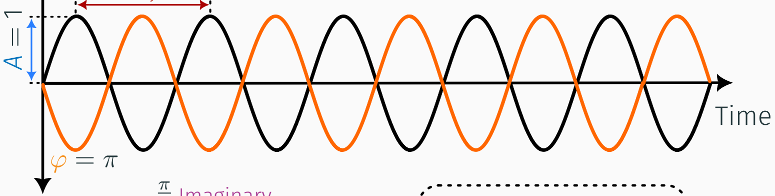

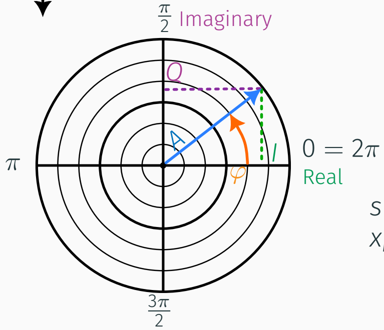

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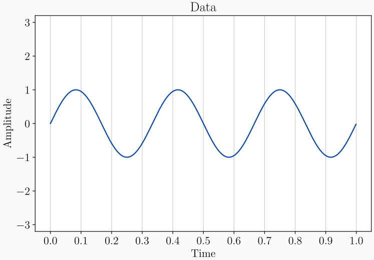
Phase Modulation (PM)



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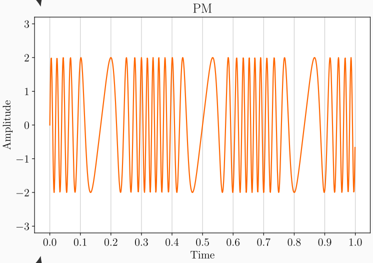
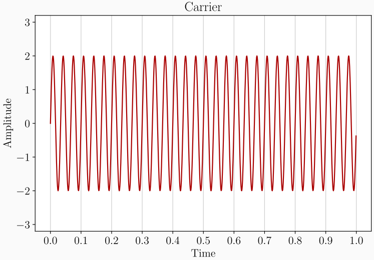


Phase-modulated carrier (Bandpass):
$y(t) = A_c \sin(2\pi f_c t + \varphi_c + m(t))$



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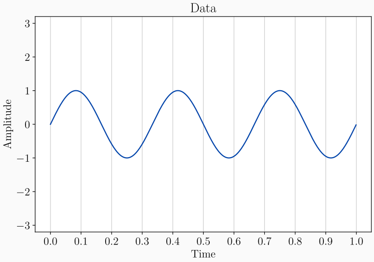

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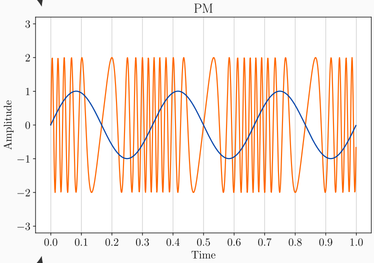
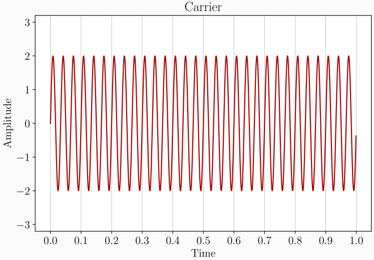
$m(t) = A_m \sin(2\pi f_m t + \varphi_m)$

Phase-modulated carrier (Bandpass):

$y(t) = A_c \sin(2\pi f_c t + \varphi_c + m(t))$





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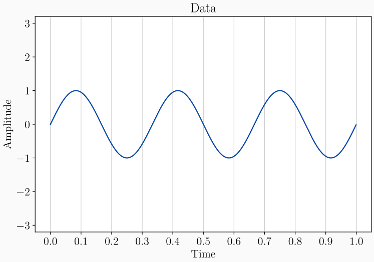
Phase Modulation (PM)



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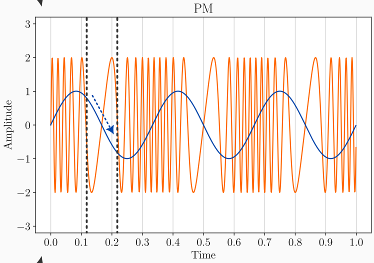

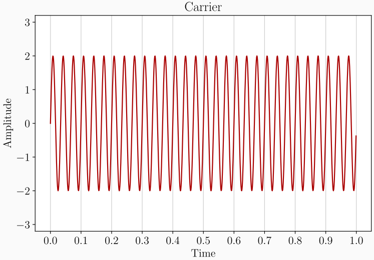

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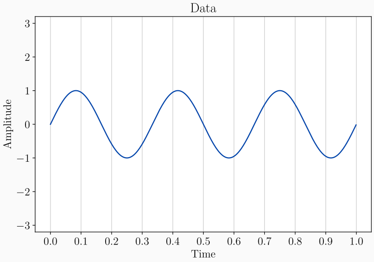

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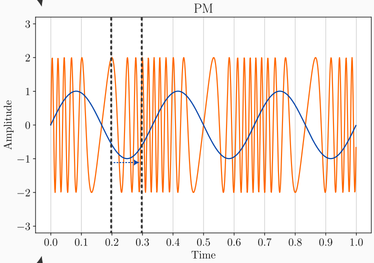

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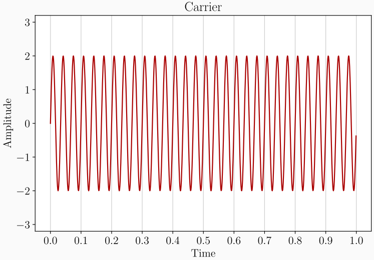

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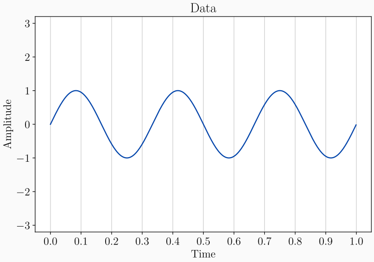

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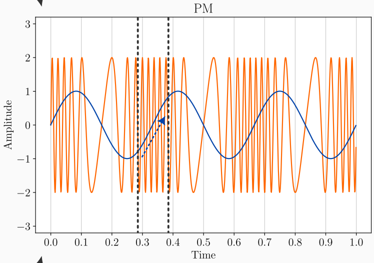

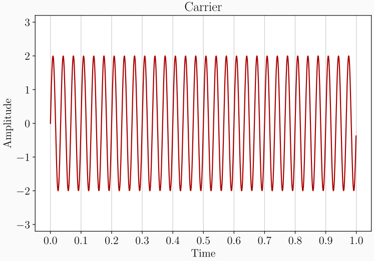

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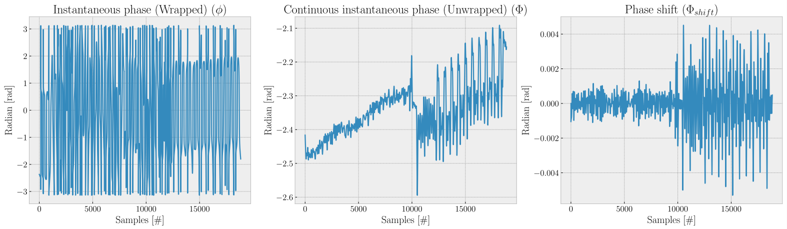
Phase Trace Computation: Step 1



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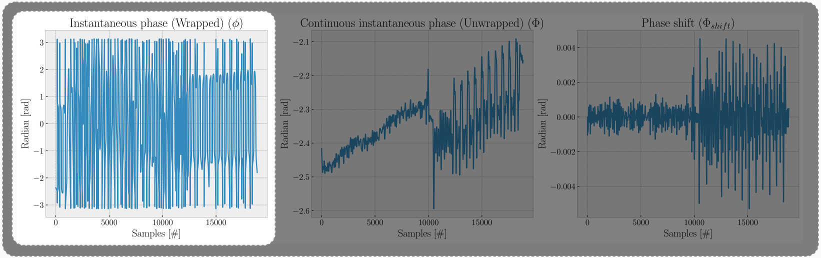
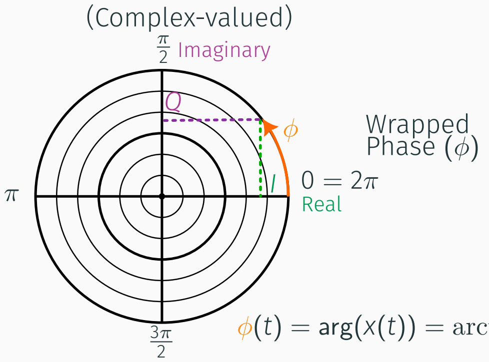


Step 1: Instantaneous Phase



$$\phi(t) = \arg(x(t)) = \mathrm{arctan2}\left(Q(t), I(t)\right)$$

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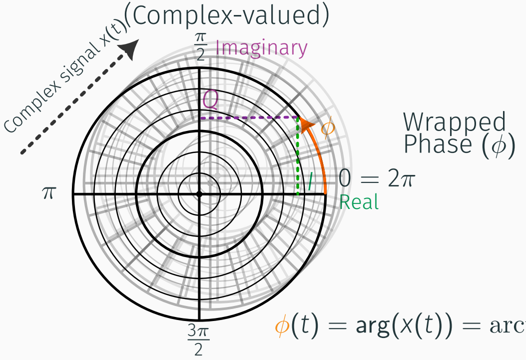

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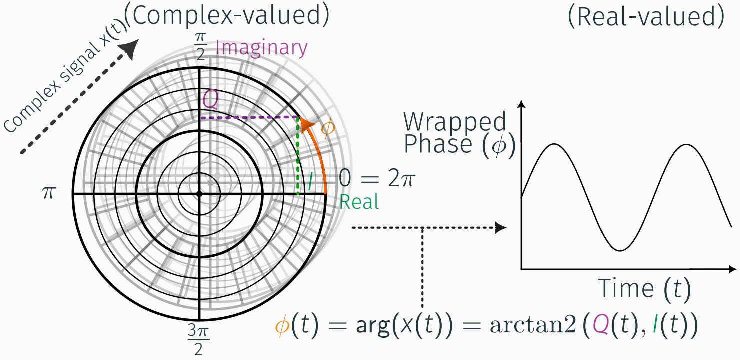

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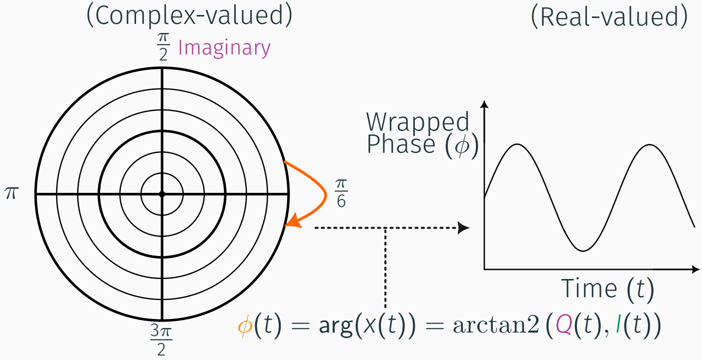

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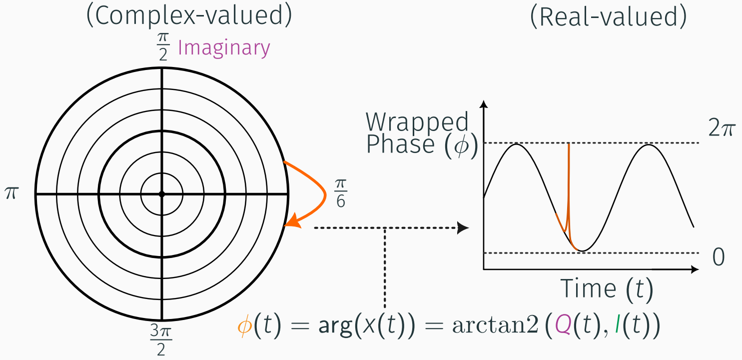
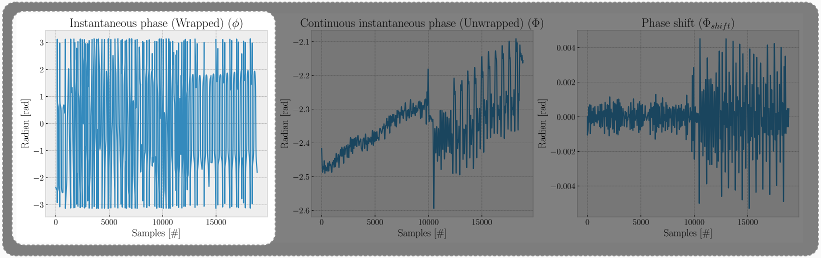


$$\phi(t) = \arg(x(t)) = \operatorname{arctan2}(Q(t), I(t))$$

Problem

- Due to cyclic nature of phase measurement, discontinuities happens in the real-valued trace
- Not comparable across measurement

Phase Trace Computation: Step 2



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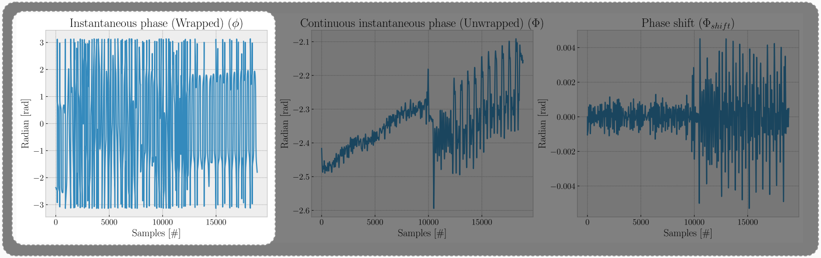
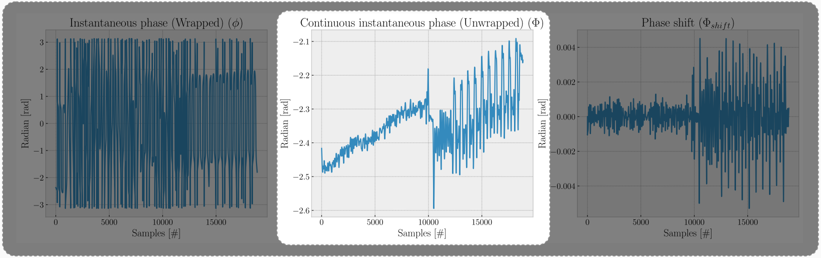


$\downarrow$



Step 2: Continuous Instantaneous Phase

$$\Phi(t) = \phi(t) + k(t)2\pi$$

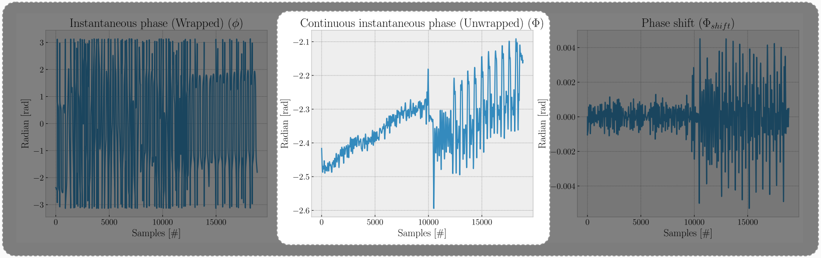
- $k \in \{0, 1, 2, ...\}$ increased for each 2π discontinuity

Step 2: Continuous Instantaneous Phase

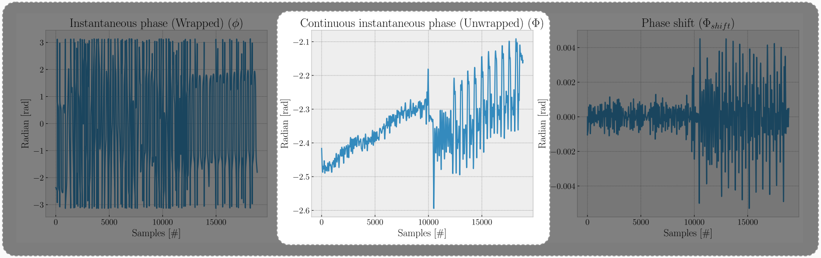
$$\Phi(t) = \phi(t) + k(t)2\pi$$

- $k \in \{0, 1, 2, \ldots\}$ increased for each 2π discontinuity
- $\Phi(t)$ cumulative function (not constrained to the 2π principal-values)

Phase Trace Computation: Step 3



Phase Trace Computation: Step 3



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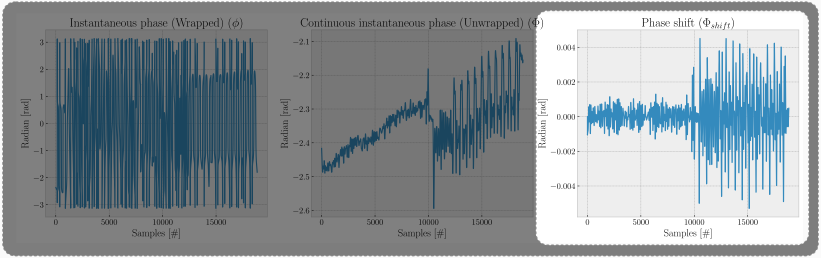
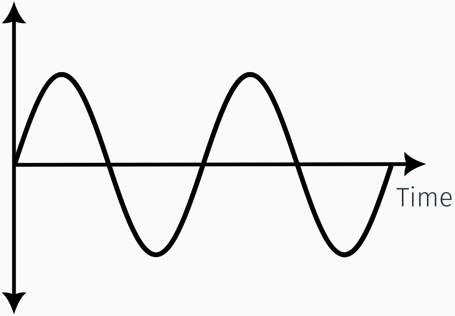


Phase Shift and Phase Rotation



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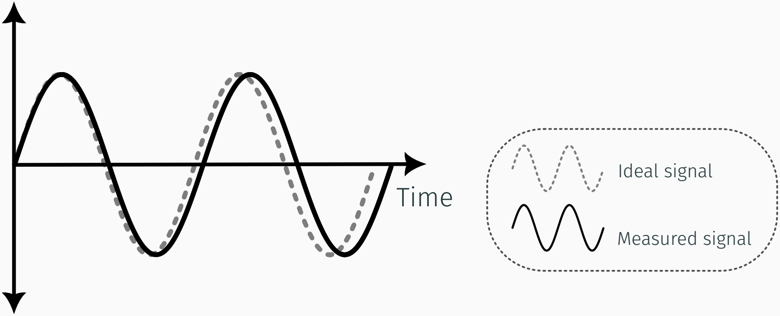

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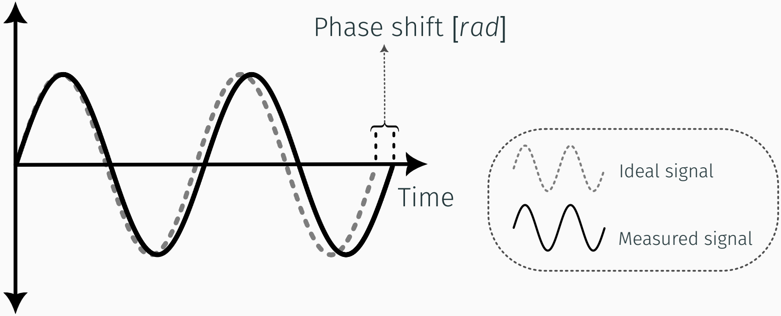

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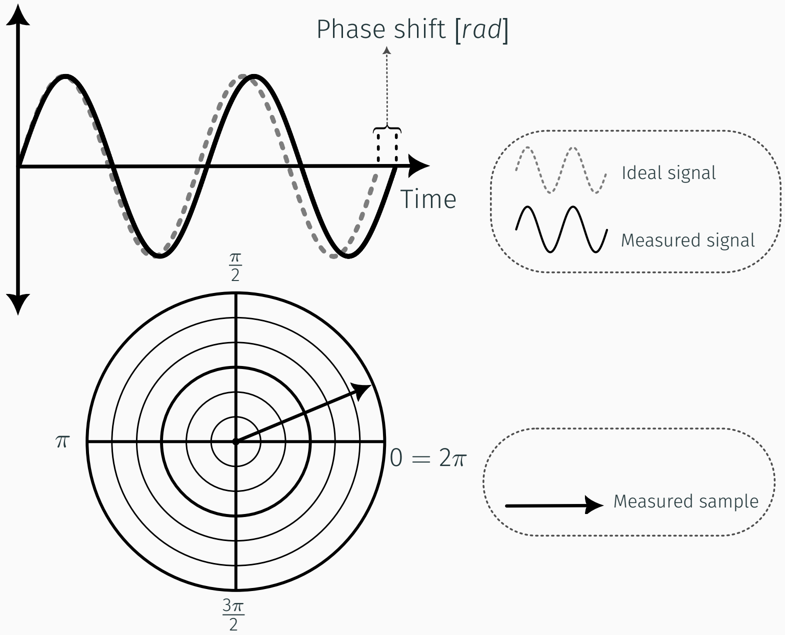

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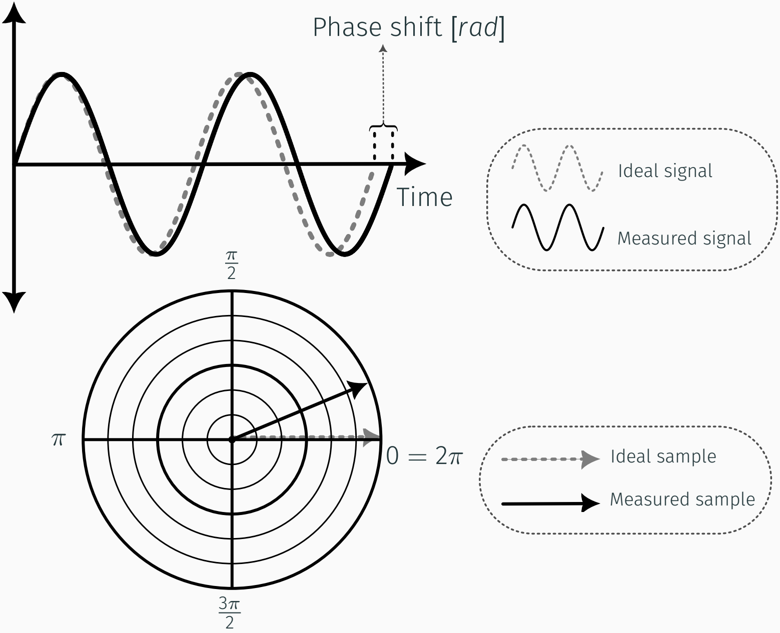

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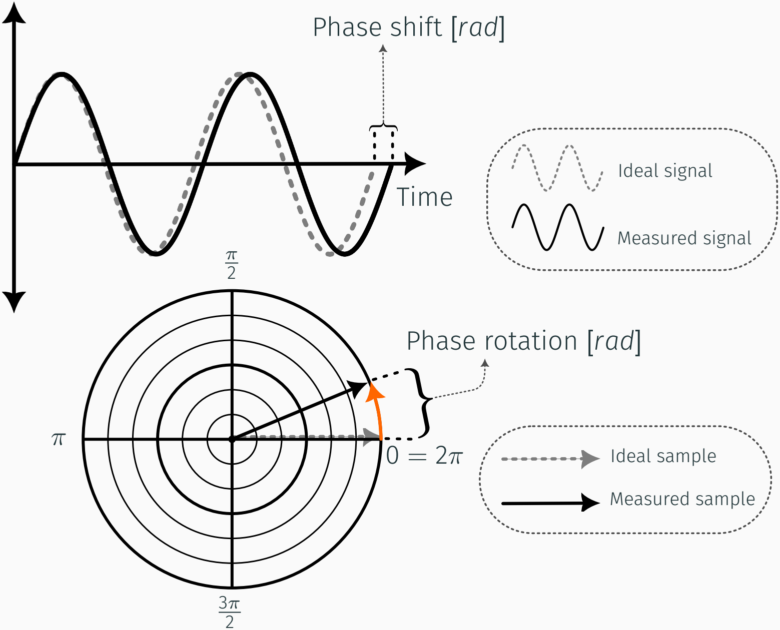
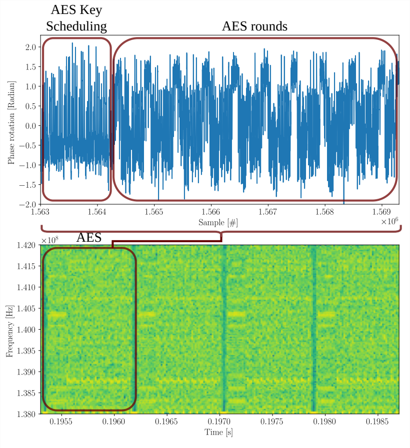


Step 3: Phase Shift Analysis

$$\Phi_{shift}(t) = \frac{d\Phi}{dt}(t) = \begin{cases} 0, & \text{if } t = 0 \\ \Phi(t) - \Phi(t-1), & \text{otherwise} \end{cases}$$

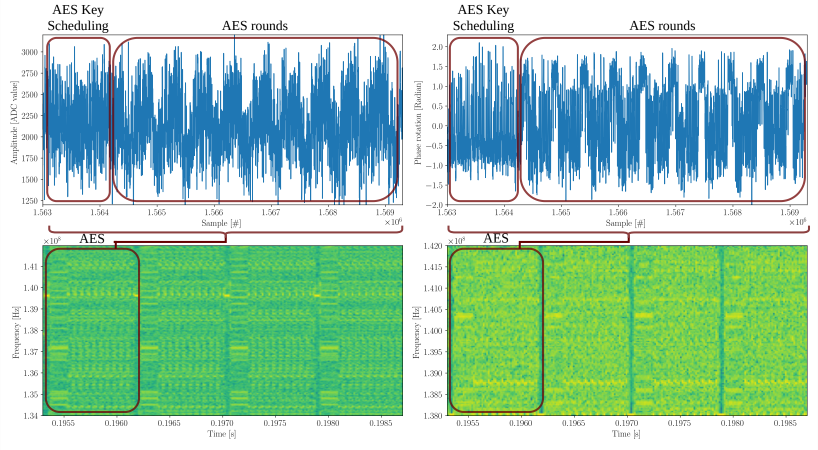
- Compute the **first derivative** (numerical differentiation)
- $\rightarrow$ Phase shift between two samples

Visualizing AES in a Phase Shift Trace



Captured from an nRF52832 using a near-field probe connected to an SDR tuned at 2^{nd} clock harmonic

Visualizing AES in a Phase Shift Trace



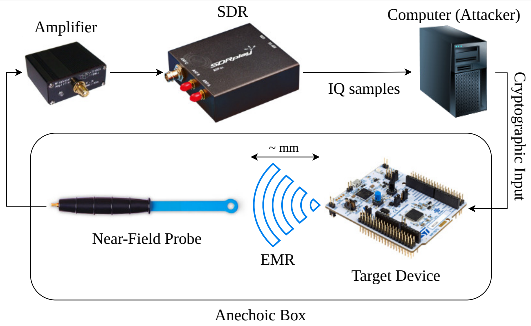
AES trace in amplitude (left) and phase shift (right)

Captured from an nRF52832 using a near-field probe connected to an SDR tuned at 2nd clock harmonic

Exploitation of Phase-modulated Side Channels

Exploitation

Experimental Setup for Side-Channel Attack

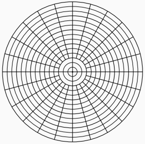


SoC	Board
STM32L1	NUCLEO-L152RE
nRF52832	PCA10040
nRF51422	PCA10028
ATmega328	Arduino Nano
RP2040	Raspberry Pi Pico

Mono-Channel Attack using Amplitude

(Complex-valued)

I/Q



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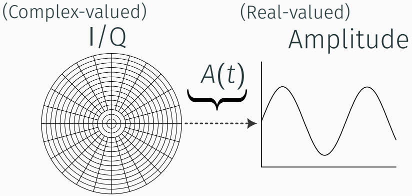

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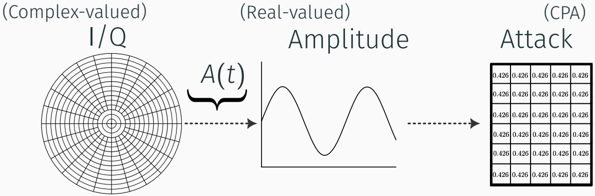
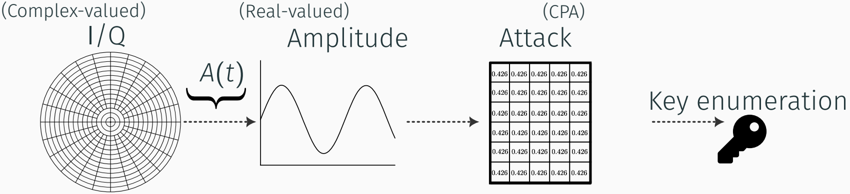
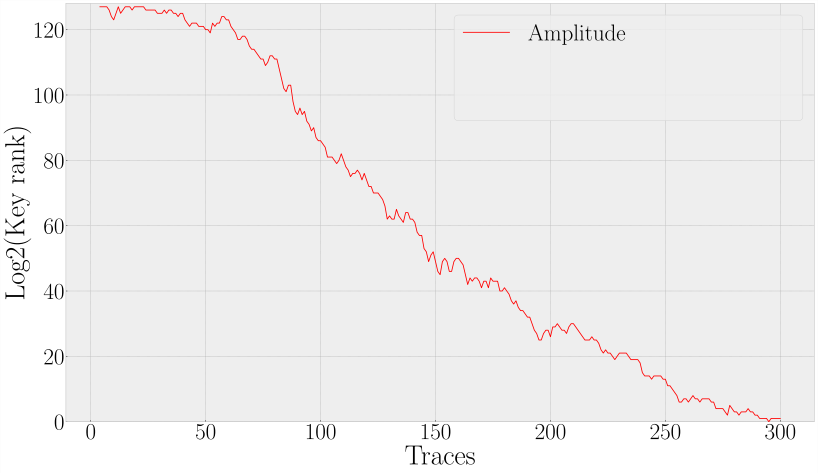


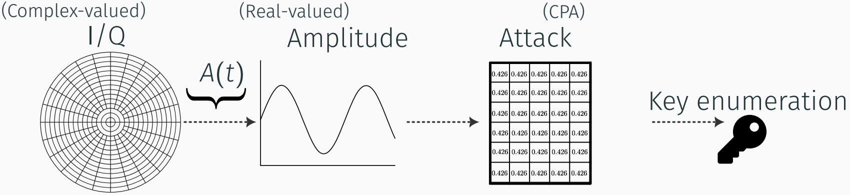
Mono-Channel Attack using Amplitude

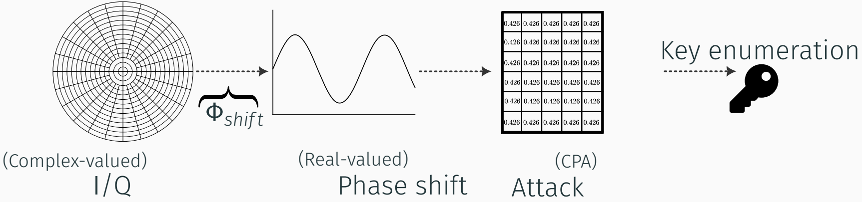


Non-Profiled Side-Channel Attack on nRF52



Mono-Channel Attack using Phase Shift





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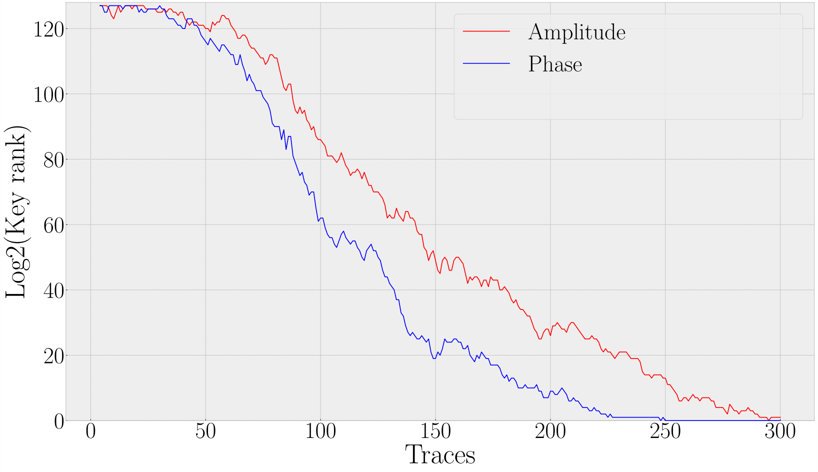

Multi-Channel Attack

Questions

1. Are the **information** on amplitude and the phase identical?

Multi-Channel Attack

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2. If not, could we recombine it?

Multi-Channel Attack

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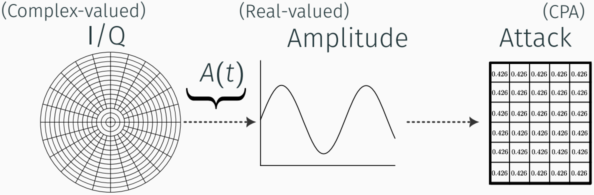
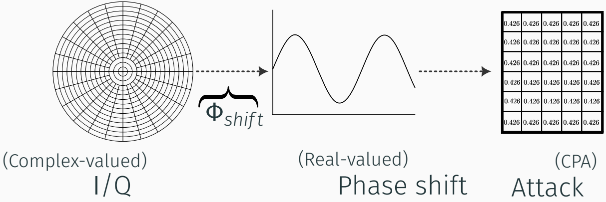
Solution

Multi-channel attacks are to side channels what diversity is to radio communications

Multi-Channel Attack





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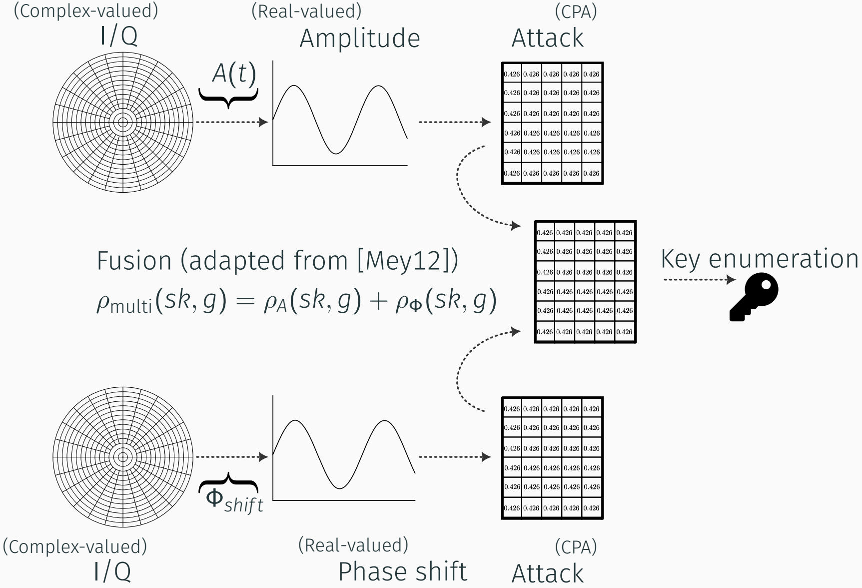
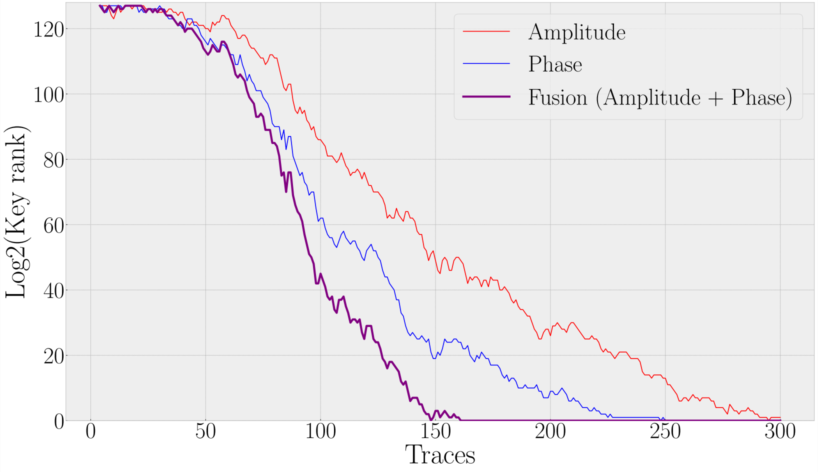


Non-Profiled Side-Channel Attack on nRF52

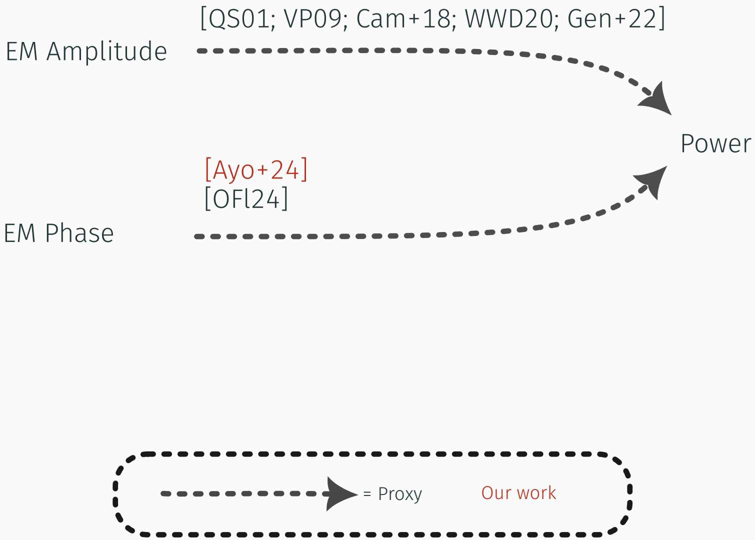


Root-cause characterization

Root-cause characterization

Hypotheses

Phase to CPU Power: Something is Missing



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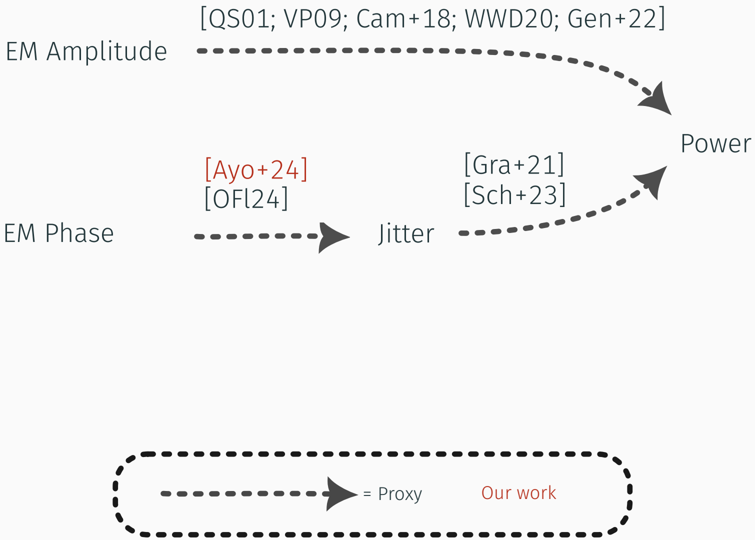
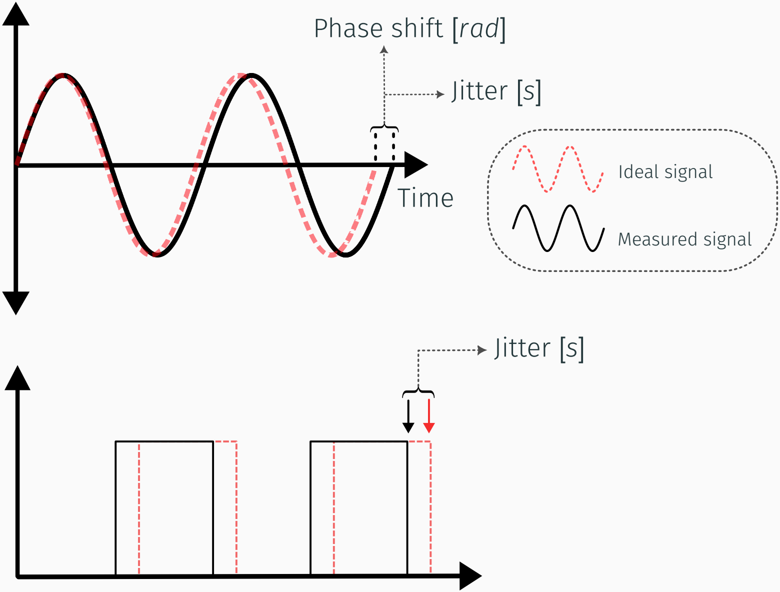


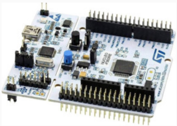
Phase to Jitter Equivalence

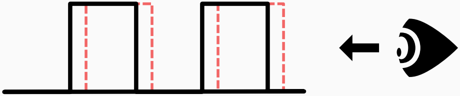


State-of-the-Art: Jitter Side-Channels

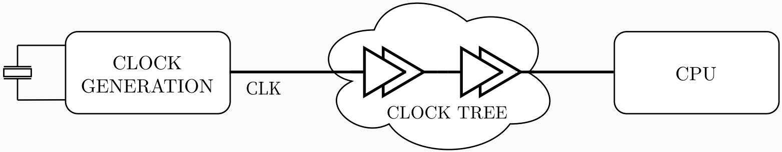
Recent Work: Timing Side Channels Exploiting Jitter

- *Gravellier et al.* [Gra+21] (2021)
  By software, they exploited the jitter correction coefficients of delay lines in high-speed digital buses (DDR).
- *Schoos et al.* [Sch+23] (2023)
  External Jitter measurement from a cryptographic target using a timing sensor at the picosecond scale.





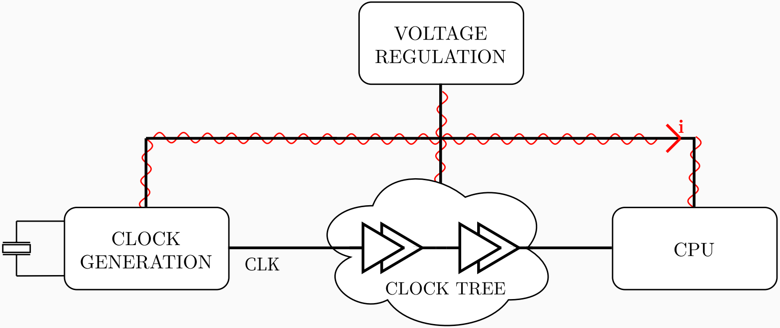
Jitter Sources Hypotheses in MCUs / SoCs



Question

- Which components are more **sensitive to noise**?

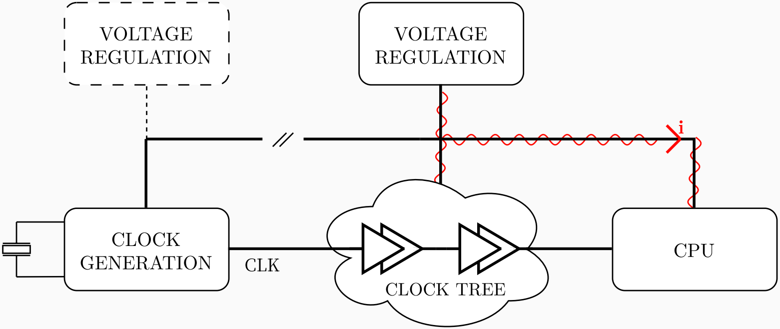
Jitter Sources Hypotheses in MCUs / SoCs



Coupling path

- **Conducted noise** via power rails

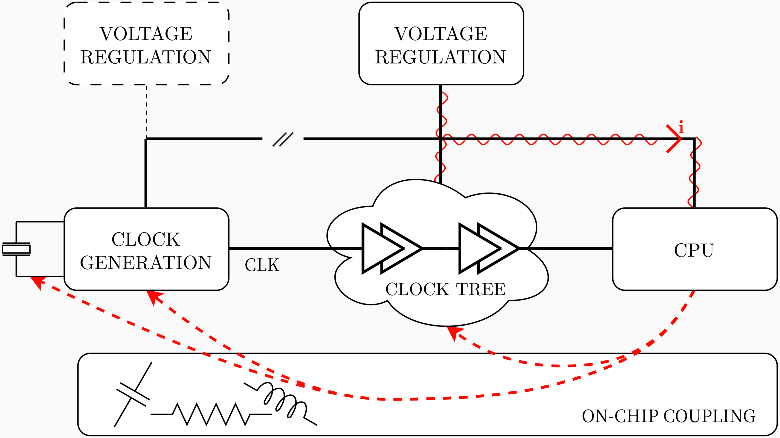
Jitter Sources Hypotheses in MCUs / SoCs



Coupling path

- But, voltage regulation subsystems may be decoupled...

Jitter Sources Hypotheses in MCUs / SoCs



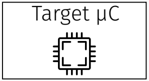
Indirect coupling because of parasitic effects

- **Resistive, capacitve and inductive** coupling

Root-cause characterization

Experiments

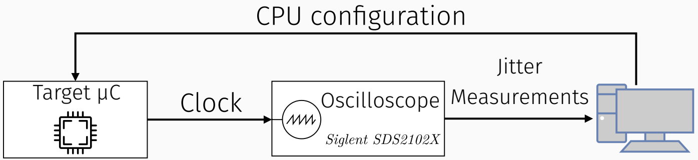
Experimental Setup for Jitter Source Study



STM32F µC familly (STM32F103)

- **Flexibility** Highly configurable internal clock generation circuit
- **Observability** Internal clocks can be routed externally

Experimental Setup for Jitter Source Study



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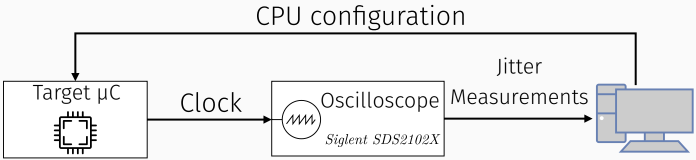
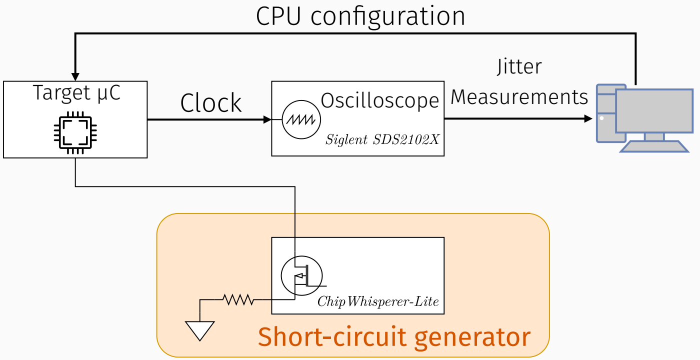


CPU Configurations

- **SLEEP** CPU powered off
- **STALL** Infinite while-loop (branching only)
- **AES** Continuous AES computation

Experimental Setup for Jitter Source Study



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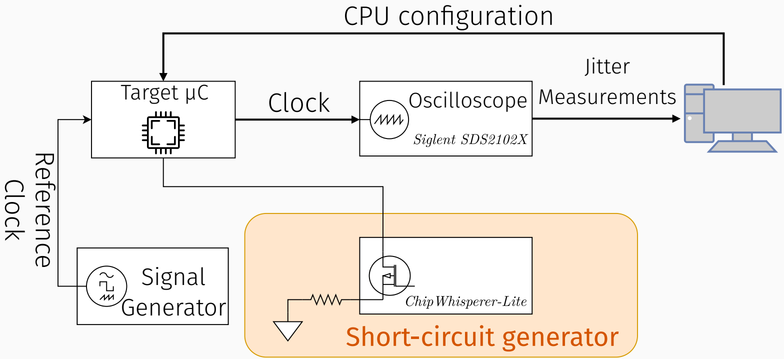
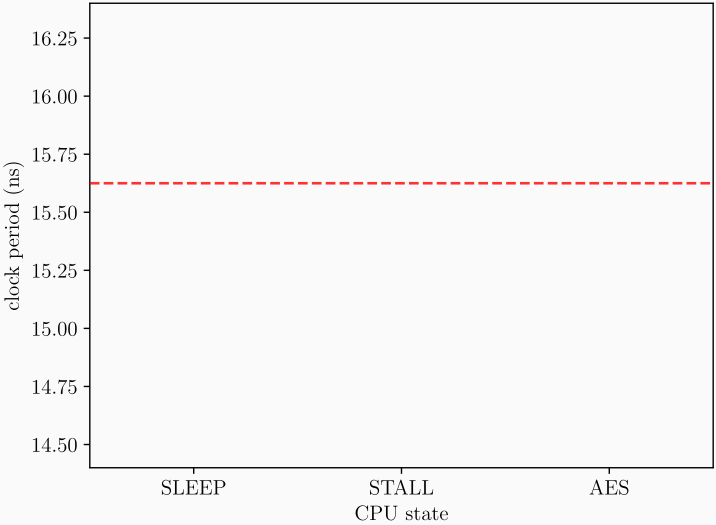
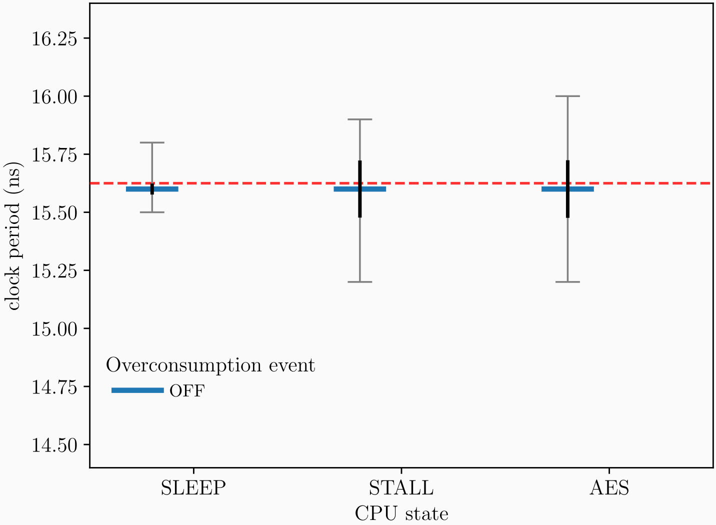


Jitter *vs.* Consumption



Clock Jitter under various power consumption conditions

Jitter *vs.* Consumption



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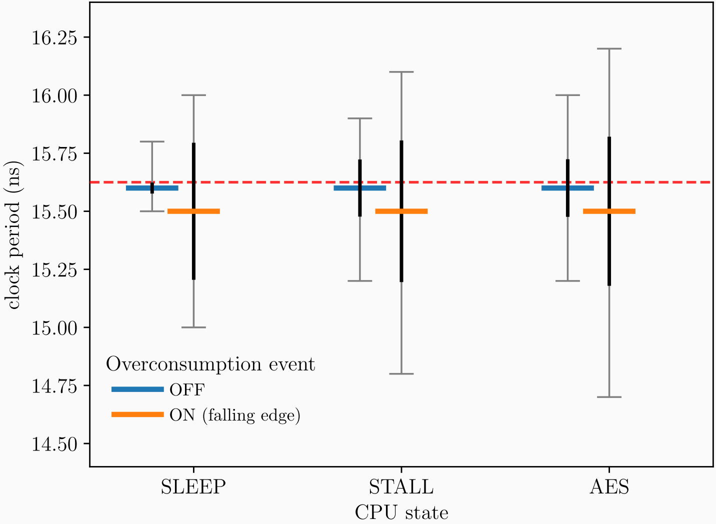

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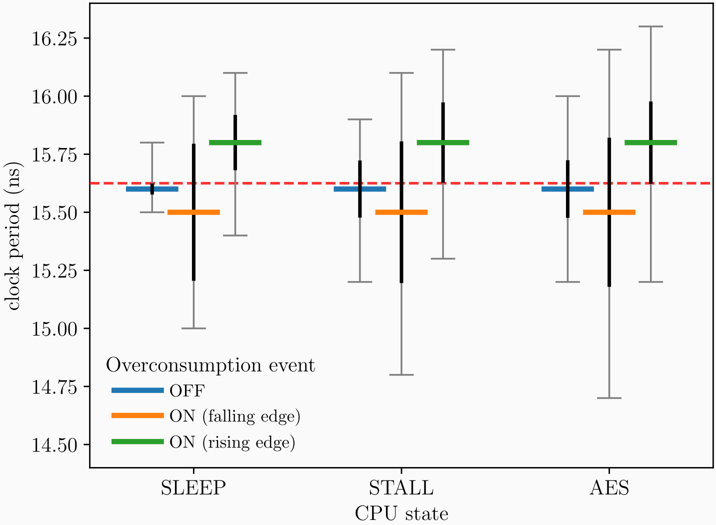
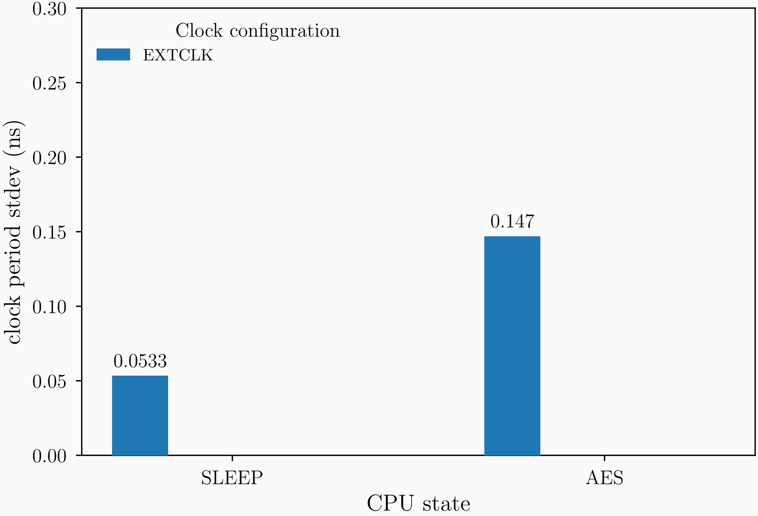


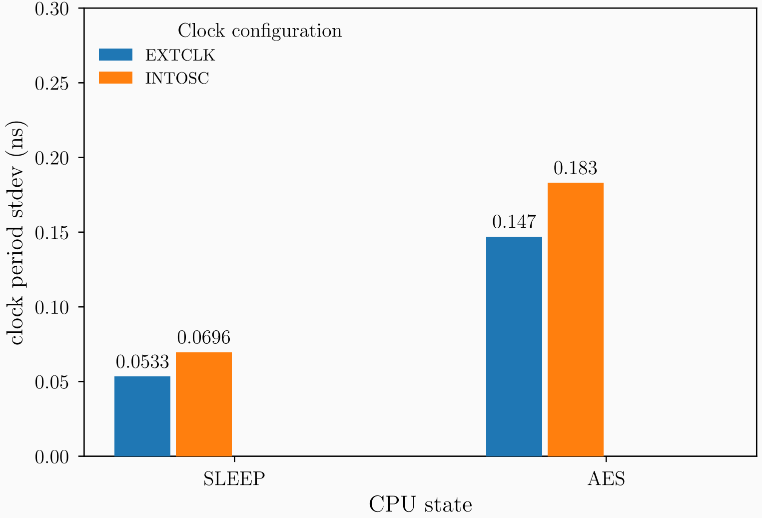
Clock Jitter under various power consumption conditions

Jitter *vs.* Clock Configuration



Clock Jitter under various internal clock circuit configurations.

Jitter *vs.* Clock Configuration



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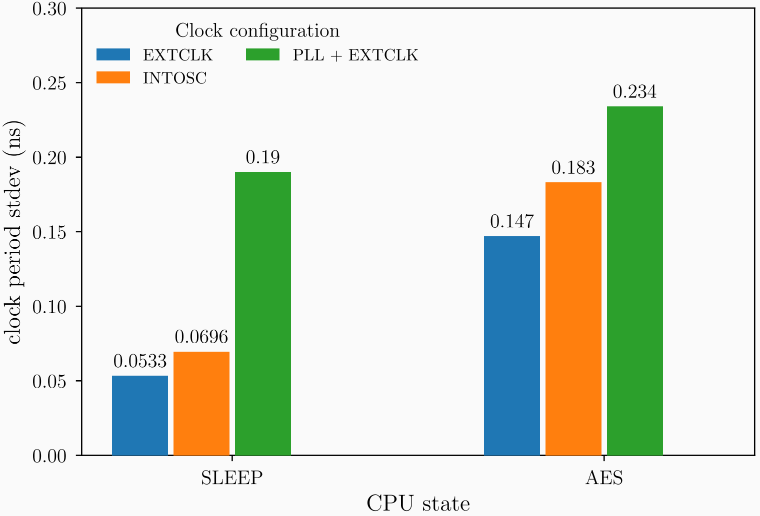

Clock Jitter under various internal clock circuit configurations.

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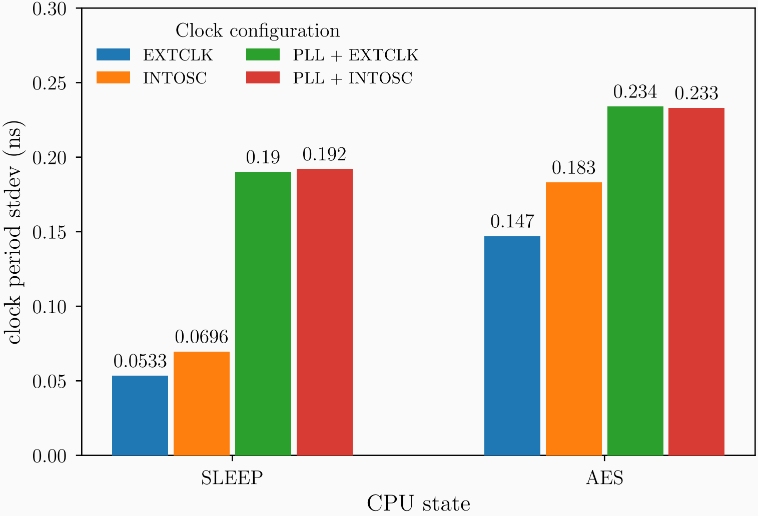
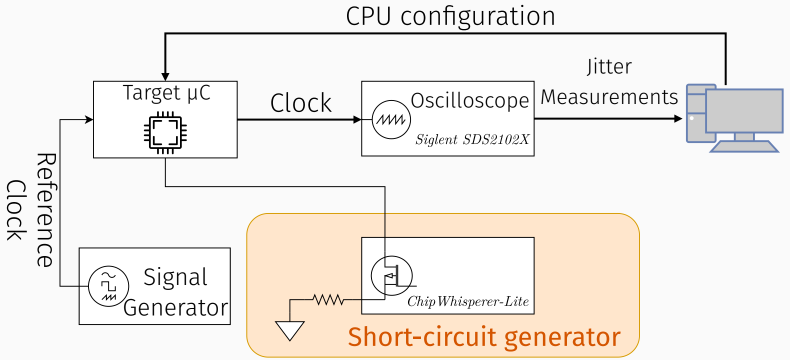


Clock Jitter under various internal clock circuit configurations.

Overconsumption Effect on EM Phase – Setup



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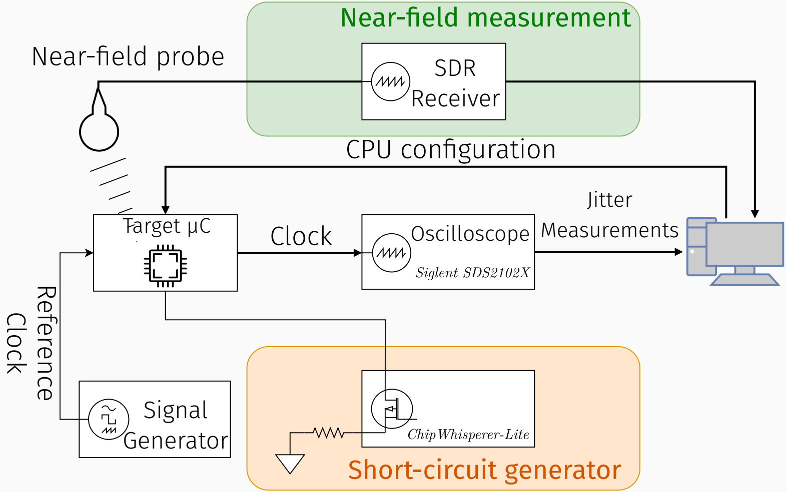
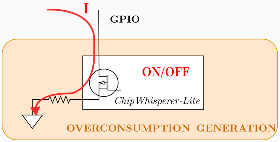
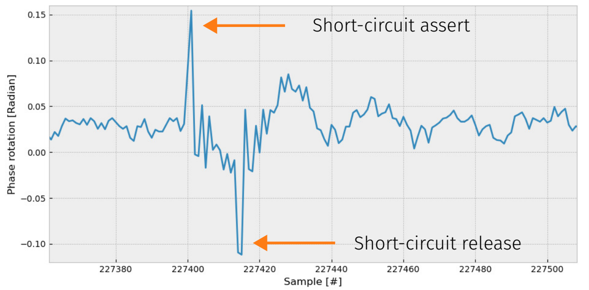
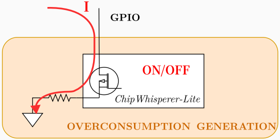


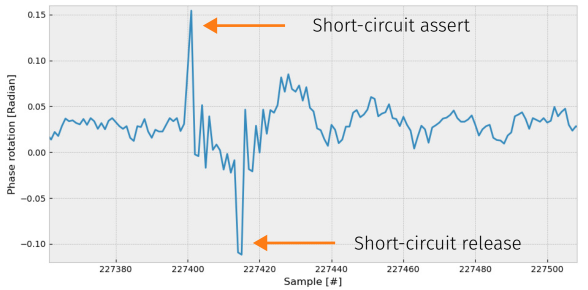
Overconsumption Effect on EM Phase – Results





Overconsumption Effect on EM Phase – Results





Measure example

- Jitter (Δt) measure: 275 ps
- Phase shift (ϕ) measure: 0.125 rad
- Jitter to Phase shift conversion: $\phi = 2\pi f \cdot \Delta t$
- Error $\approx$ 0.014 rad

Conclusion

Attacks Summary

SoC	Key Recovery using Amplitude / Phase Shift
STM32L1	✔ / ✔
nRF52832	✔ / ✔
nRF51422	✔ / ✔
ATmega328	✔ / ✔
RP2040	✘ / ✘

Lots of devices seems to be impacted...

Conclusion

Questions

May systems not vulnerable to **amplitude EM analysis** be vulnerable to **phase EM analysis**?

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Future work

Assess how **SDR** performs compared to **oscilloscope** using MCFA

Conclusion

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May systems not vulnerable to **amplitude EM analysis** be vulnerable to **phase EM analysis**?

Future work

Assess how **SDR** performs compared to **oscilloscope** using MCFA

Practical applications

Attacks suffering from limited performance with amplitude may become threatening with phase

Questions?

Pierre Ayoub, Aurélien Hernandez, Romain Cayre, Aurélien Francillon, Clémentine Maurice "PhaseSCA: Exploiting Phase-Modulated Emanations in Side Channels". In: *IACR Transactions on Cryptographic Hardware and Embedded Systems (TCHES)*, 2024

Artifact (Code & Datasets):

`https://github.com/pierreay/phasesca`

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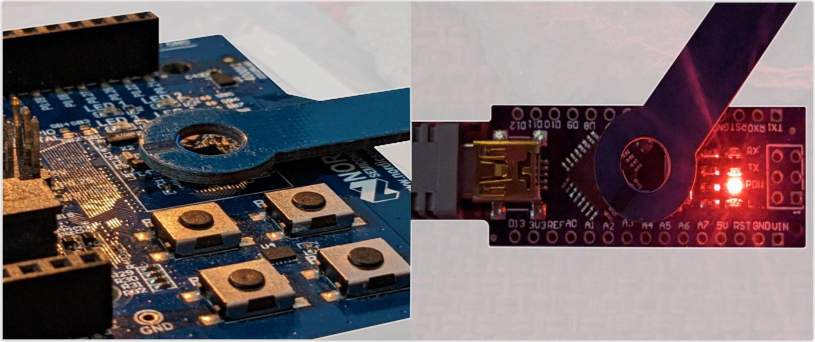
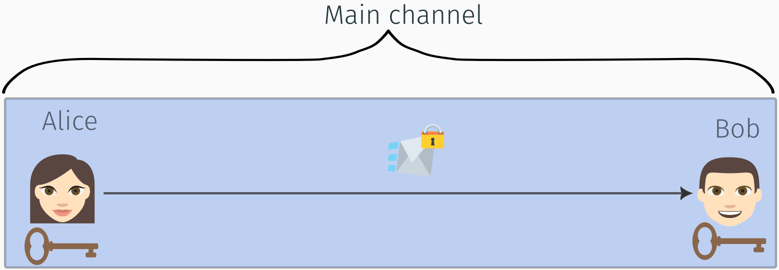
Backup Slides

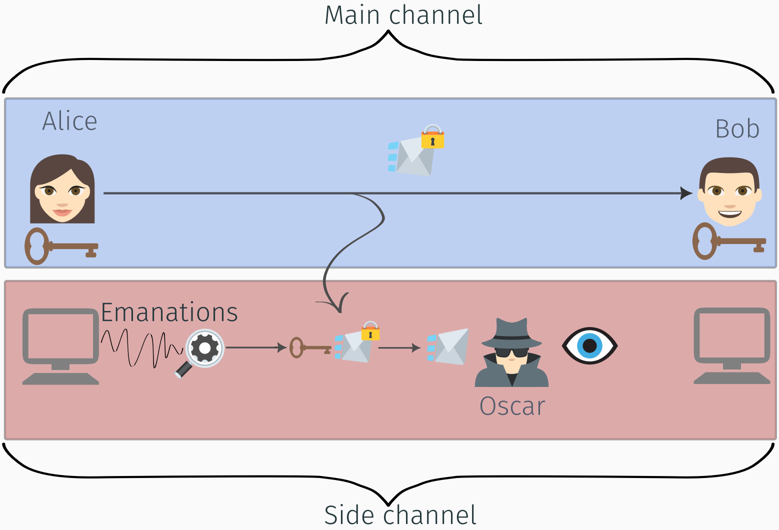
Measuring EM emanations



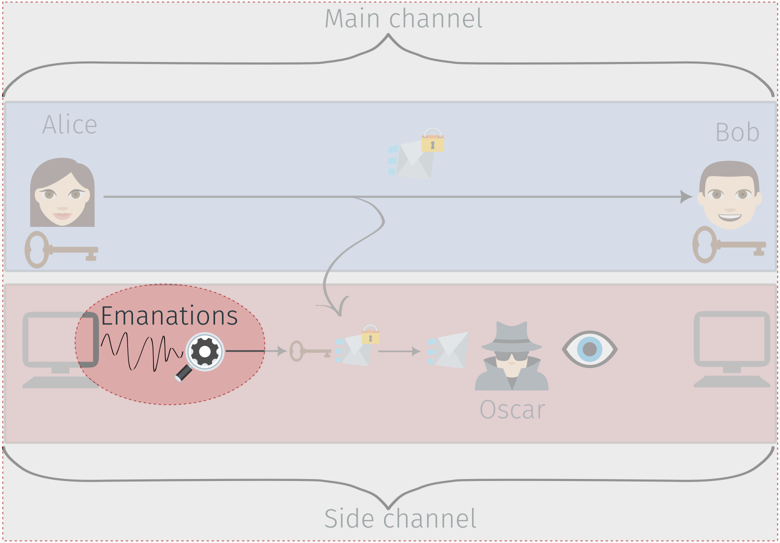
Main channel *vs.* Side channel



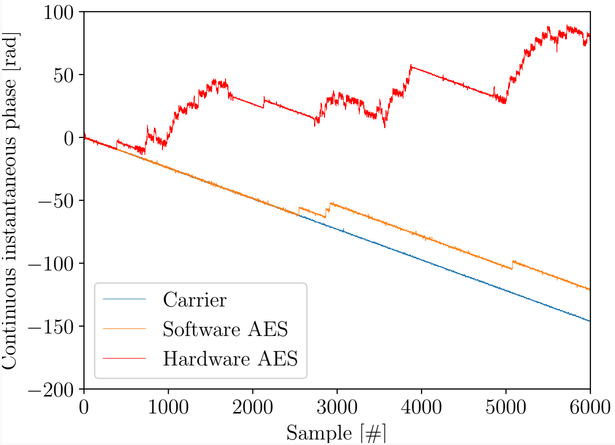
Main channel *vs.* Side channel



Main channel *vs.* Side channel



Identifying Phase-Modulated Leakage on a Target SoC



Filtering the Leaked Signal: Principle

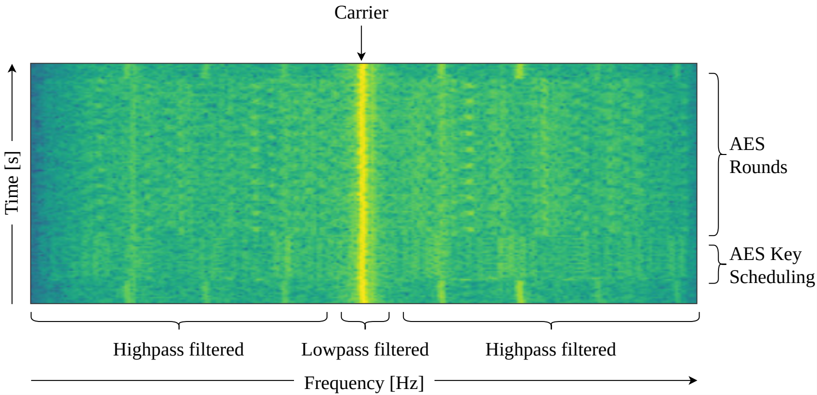
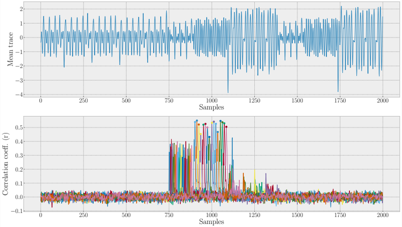
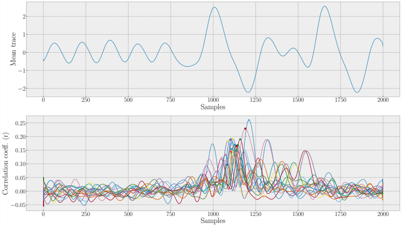


Figure 1: Waterfall illustrating filters isolating amplitude and phase shift leakage. A low-pass filter is used to isolate the phase-modulated leakage, while a high-pass filter is used to isolate the amplitude-modulated leakage.

Filtering the Leaked Signal: Results



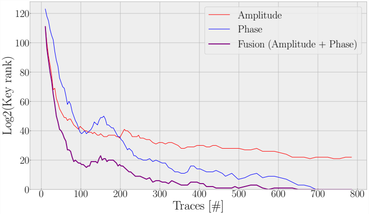
(a) Using a low-pass filtered signal at 1 MHz.



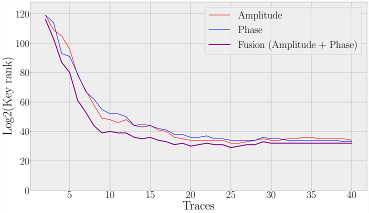
(b) Using a low-pass filtered signal at 50 kHz.

Figure 2: Correlation coefficients (ρ) for POIs on phase shift for the nRF52.

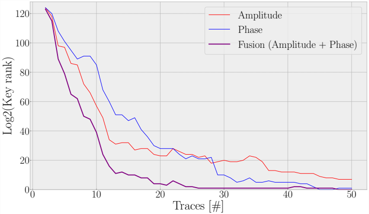
Performance for Profiled Attacks



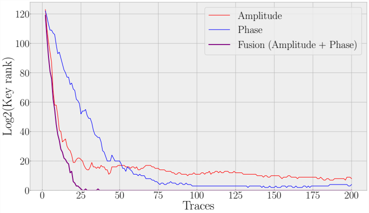
(a) Key rank for the nRF52.



(b) Key rank for the nRF51.

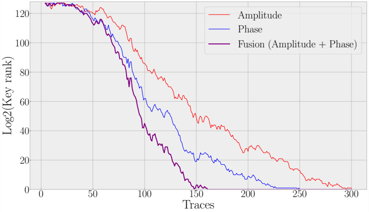


(c) Key rank for the STM32L1.

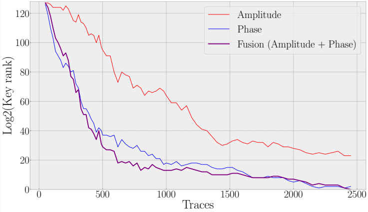


(d) Key rank for the ATmega328.

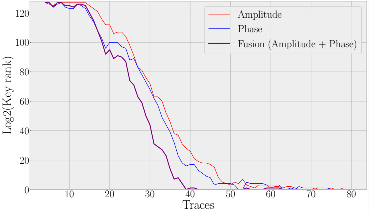
Performance for Non-Profiled Attacks



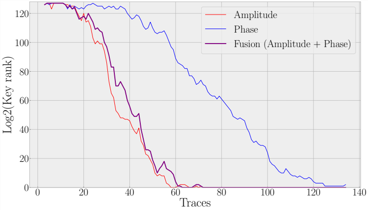
(a) Key rank for the nRF52.



(b) Key rank for the nRF51.

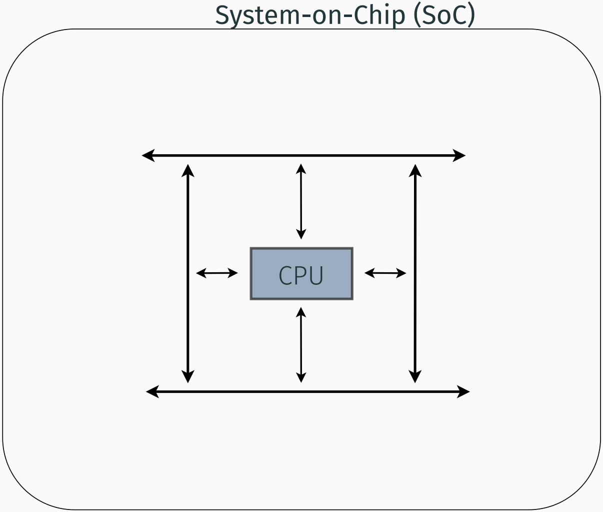


(c) Key rank for the STM32L1.



(d) Key rank for the ATmega328

Embedded System Complexity is Increasing



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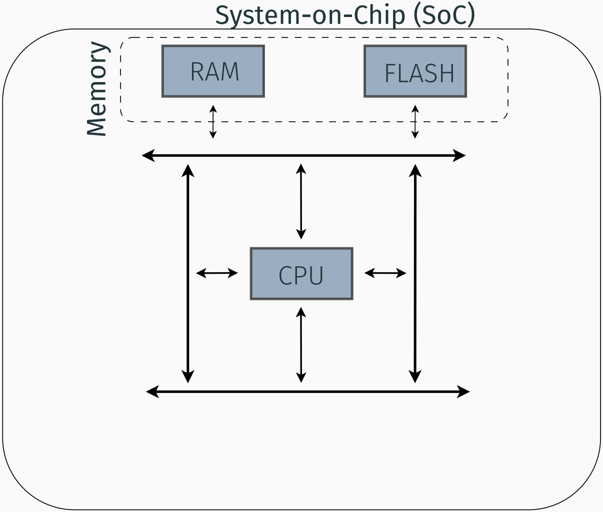

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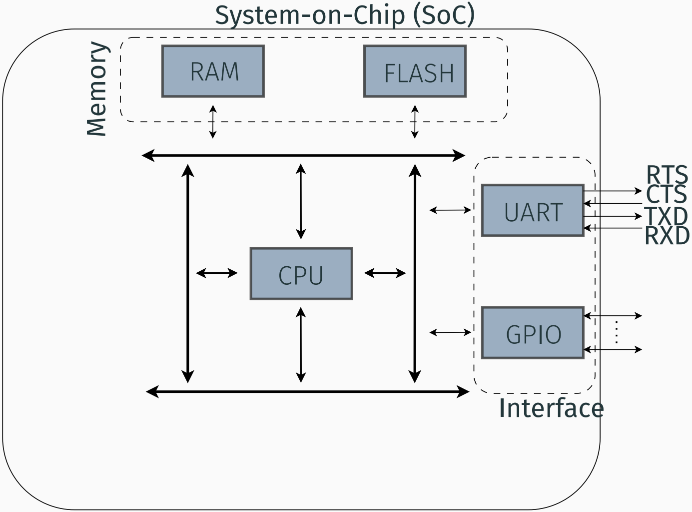

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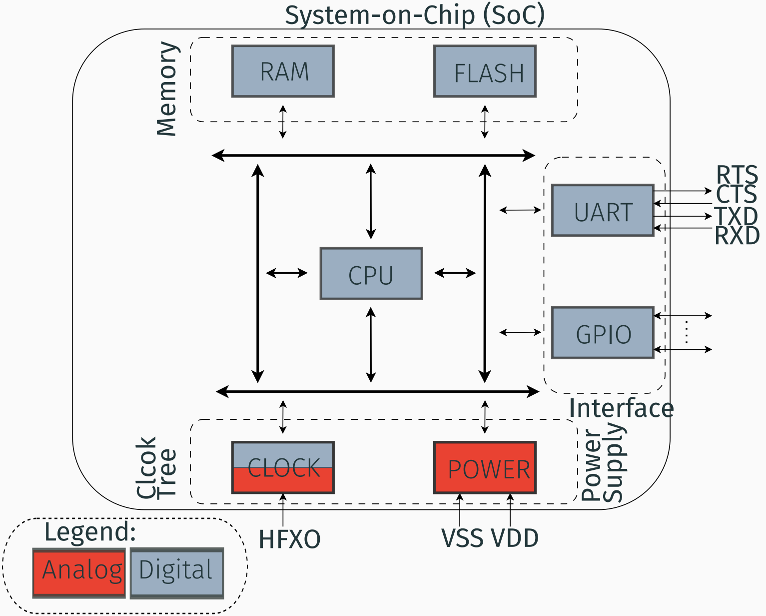

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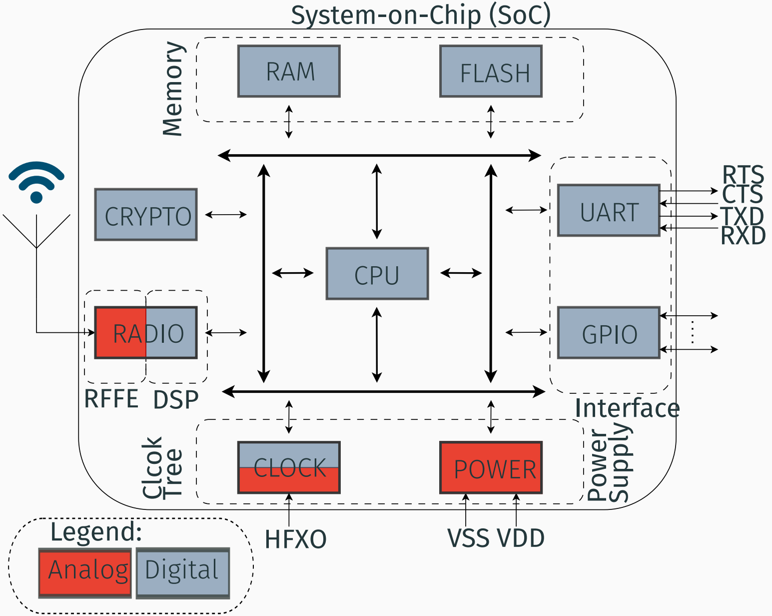

Phase in Screaming Channels (Custom)

AES leak signal at Screaming Channels frequencies in the Far Field (FF) 2.5 GHz).

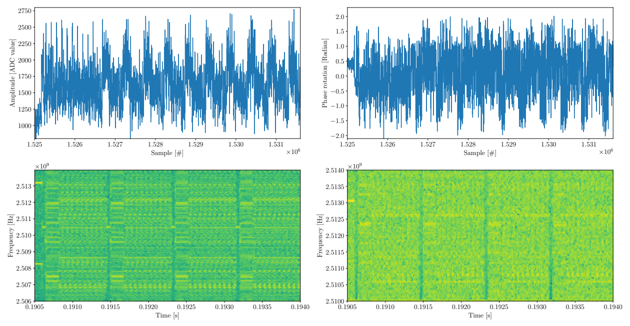

Figure 5: Signal captured during radio broadcast from an instrumented firmware in both time-domain (upper) and frequency-domain (down) for both amplitude (left) and phase (right). We can observe the key scheduling of AES and its 10 rounds in time-domain and 4 full run of AES in frequency-domain.

Phase in Screaming Channels (NimBLE)

AES leak signal at Screaming Channels frequencies in the Far Field (FF) 2.5 GHz).

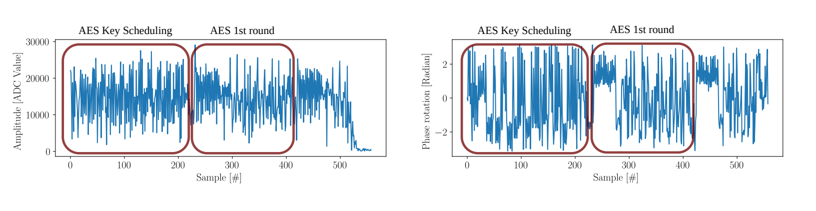

Figure 6: Signal captured during a BLE communication from NimBLE for both amplitude (left) and phase (right).

Zoom on a Example Clocking Circuit

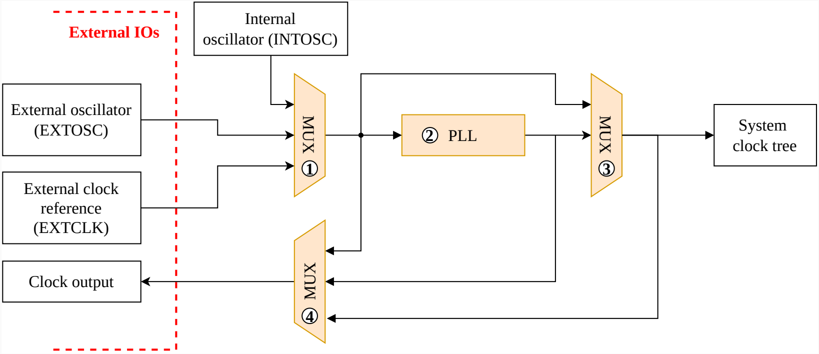

Figure 7: Simplified view of the STM32F103RB internal clocking circuit.

Countermeasures

Physical

- Filtering
- Shielding
- Grounding
- Decoupling
- PCB Design

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- Grounding
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Cryptography

- Masking
- Hiding

State-of-the-Art

Foundational Work: EM Side Channels

- *NSA's NACSIM 5000: TEMPEST Fundamentals* [Ros82]
- *Agrawal et al.* [Agr+03]: Preliminary experiments with PM/FM emanations
- *Li et al.* [LMM05]

State-of-the-Art

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Recent Work: Timing Side Channels exploiting Jitter

- *Gravellier et al.* [Gra+21]: Read delay-line registers
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State-of-the-Art

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Parallel Work: Side Channels exploiting Phase Modulation

- *Colin O'Flynn* [OFl24]: Physical connection to RF mixer

Root Causes

- Due to **complexity of chip designs**, results must be treated with precaution

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